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NOTES:  
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

CPU LIST			
I3-1005G1	ICL	6025B0405601	SRGKF
I5-1035G1	ICL	6025B0404801	SRGKG
I7-1065G7	ICL	6025B0407701	SRGON

GPU LIST		
AMD R19M-M18-30	GDDR5 216-0915020	6019B1961001

VRAM LIST		
Hynix	H5GC8H24MJR-R0C	6019B1542101
Micron	MT51J256M32HF-70:A	6019B1486001
Samsung	K4G80325FB-HC28	6019B1485901
Hynix	H5GC8H24AJR-R2C A	6019B1723701
Micron	MT51J256M32HF-80:B B	6019B1721101
Samsung	K4G80325FC-HC25	6019B1926601

HEDWIG

INTEL ICE LAKE-U 15W

DIS : 24.5X24.5

GPU : AMD R19M-M18-30

VRAM : GDDR5 256MX32X2PCS

MV BUILD 2020.01.07

SSID  
UMA 868C  
DIS 868D

LOCATION	LEVEL		CO-LAY
PAD6015	PVBAT	SHORT	
PAD60200	P5V0A	SHORT	
PAD60210	PVBAT	SHORT	
PAD60100	P3V3A	SHORT	
PAD60110	PVBAT	SHORT	
PAD60103	P3V3AL	SHORT	
PAD60310	PVBAT	SHORT	
PAD60300	P1V2	SHORT	
PAD60350	P0V6S	SHORT	
PAD6970	P1V8A	SHORT	R6979 OPEN
PAD6980	P5V0A	SHORT	
PAD66020	PVBAT	SHORT	
PAD66010	PVBAT	SHORT	
PAD66610	PVBAT	SHORT	
PAD60410	P3V3A	SHORT	
PAD3000	PVBAT	OPEN	F3033 SHORT
PAD67010	PVBAT	SHORT	
PAD67200	P1V35S_DGPU	SHORT	
PAD67210	PVBAT	SHORT	
PAD67500	PVPCIE	SHORT	
PAD67510	P3V3A	SHORT	
PAD67410	P3V3A	SHORT	
PAD67400	P1V8S_DGPU	SHORT	
PAD1700	P5V0S	SHORT	
PAD1900	P3V3S_SSD	SHORT	

MV\_0102

ID PIN FOR BIOS

MV\_1225

PROJECT_ID	R42 15W	U22 15W
R4612	MOUNT	OPEN
R4611	OPEN	MOUNT
	3V	0V

BOARD_ID2	M18-70	M18-30
R4617	MOUNT	OPEN
R4618	OPEN	MOUNT
	3V	0V

GPU_PRINTE	UMA	DIS
R4615	MOUNT	OPEN
R4614	OPEN	MOUNT
	3V	0V

GPU_PYWRK	UMA	DIS
	MOUNT	OPEN

BUILD_ID	ID1 00000000	ID0 00000000
DB	0	0
SI	0	1
PV	1	0
MV	1	1

BOARD_ID0	17	14
R4616	MOUNT	OPEN
R4620	OPEN	MOUNT
	3V	0V

BOARD_ID1	VRAMF4	VRAMF2
R4619	MOUNT	OPEN
R4621	OPEN	MOUNT
	3V	0V

WWAN_SKU_ID	WWAN	Non-WWAN
R4622	MOUNT	OPEN
R4623	OPEN	MOUNT
	3V	0V

ID PIN FOR EC

MV\_1225

GPU_UMA_SEL	DIS	UMA
R362	MOUNT	OPEN
R363	OPEN	MOUNT
	3V	0V

Phase_ID	SI	DB	PV / MV
R337	10K_short	10K_short	10K_open
R322	10K_open	10K_short	10K_short
	3V	1.5V	0V

GPU_ID	M18-70	M18-30
R390	MOUNT	OPEN
R391	OPEN	MOUNT
	0V	0V

EC_PROJECT_ID	SNAPE17	GRANGER14
R310	10K_short	10K_open
R311	10K_open	10K_short
	3V	0V

ADP_SEL	65W	45W
R307	MOUNT	OPEN
R309	OPEN	MOUNT
	3V	0V

CPU_ID	R42 15W	U22 15W
R343	MOUNT	OPEN
R338	OPEN	MOUNT
	3V	0V

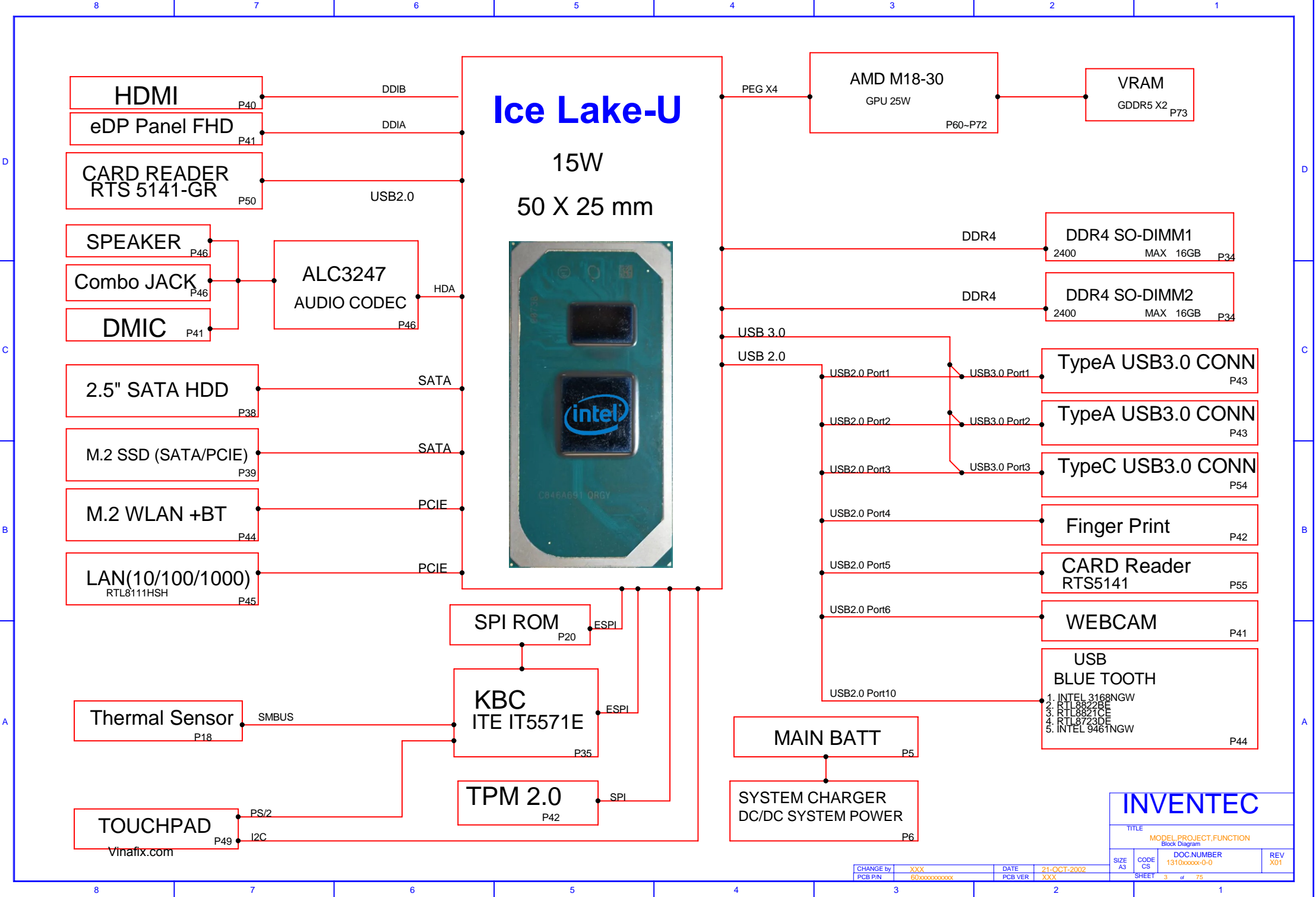
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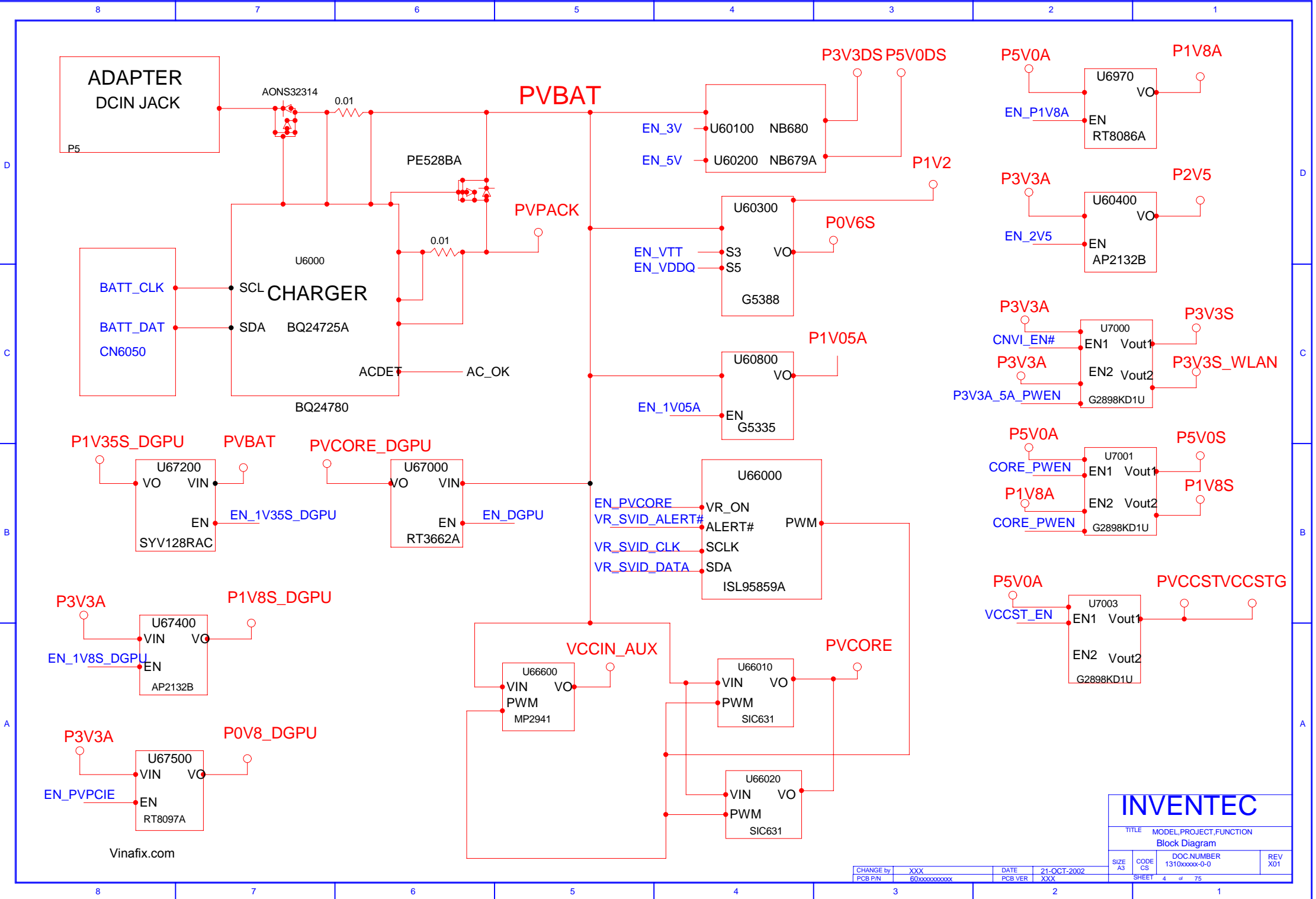
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CARD READER BOARD (TYPE C) 6050A3164201 (8L)

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11 P2V5\_AP2132B  
12 P1V8A\_RT8068A  
13 CPU VR CONTROLLER RT3613EE  
14 VCORE MOS  
15 PVCCIN AUX MP2941  
16 POWER LOAD SW  
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37 EC  
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39 SATA HDD  
40 SSD\_M2\_2280\_S3\_M-KEY  
41 HDMI  
42 30PIN LCM  
43 TPM 2.0 & FINGER PRINTER  
44 USB3.0 CONN\_2 PORT  
45 WLAN\_M2\_2230\_E-KEY  
46 AUDIO CODEC  
47 LAN\_RTL8111HSH  
48 TRANSFORMER & RJ45  
49 EMC CAP  
50 RF SOLUTION  
51 MB TO DB CONN & SCREW  
52 MB TO CR BOARD  
53 DB COVER  
54 DB1-USB3.0  
55 DB1-USB3.0 HUB  
56 DB1-USB3.0 TYPE\_C  
57 DB1-CARD READER  
58 DB1-POWER BUTTON & LID  
59 DB2-PICK BUTTON  
60 GPU COVER  
61 PVCORE\_DGPU (RT3662A)  
62 PVCORE\_DGPU MOS  
63 P1V35S\_DGPU (SYV128RAC)  
64 P1V8S\_DGPU (AP2132B)  
65 P0V8S\_DGPU (RT8097A)  
66 DGPU POWER SEQUENCE  
67 GPU-PCIE  
68 GPU-MEMORY  
69 GPU-VGA/LVDS/DVI/HDMI/DP  
70 GPU-CLOCK/JTAG  
71 GPU-THERMAL/DEBUG/GPIO/I2C  
72 GPU-POWER/GND  
73 VRAM PRO-1  
74 VRAM\_ID



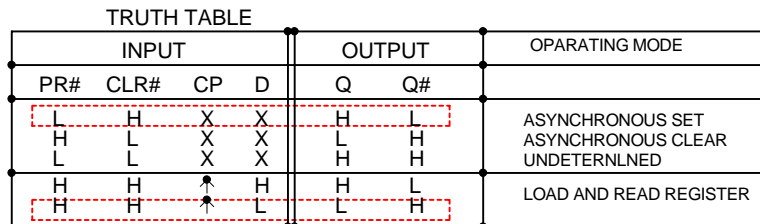


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PCB P/N	60xxxxxxxxxx	PCB VER	XXX

VER.01\_20170918



## INVENTEC

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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PCB P/N	60xxxxxxxxxx	PCB VER	XXX

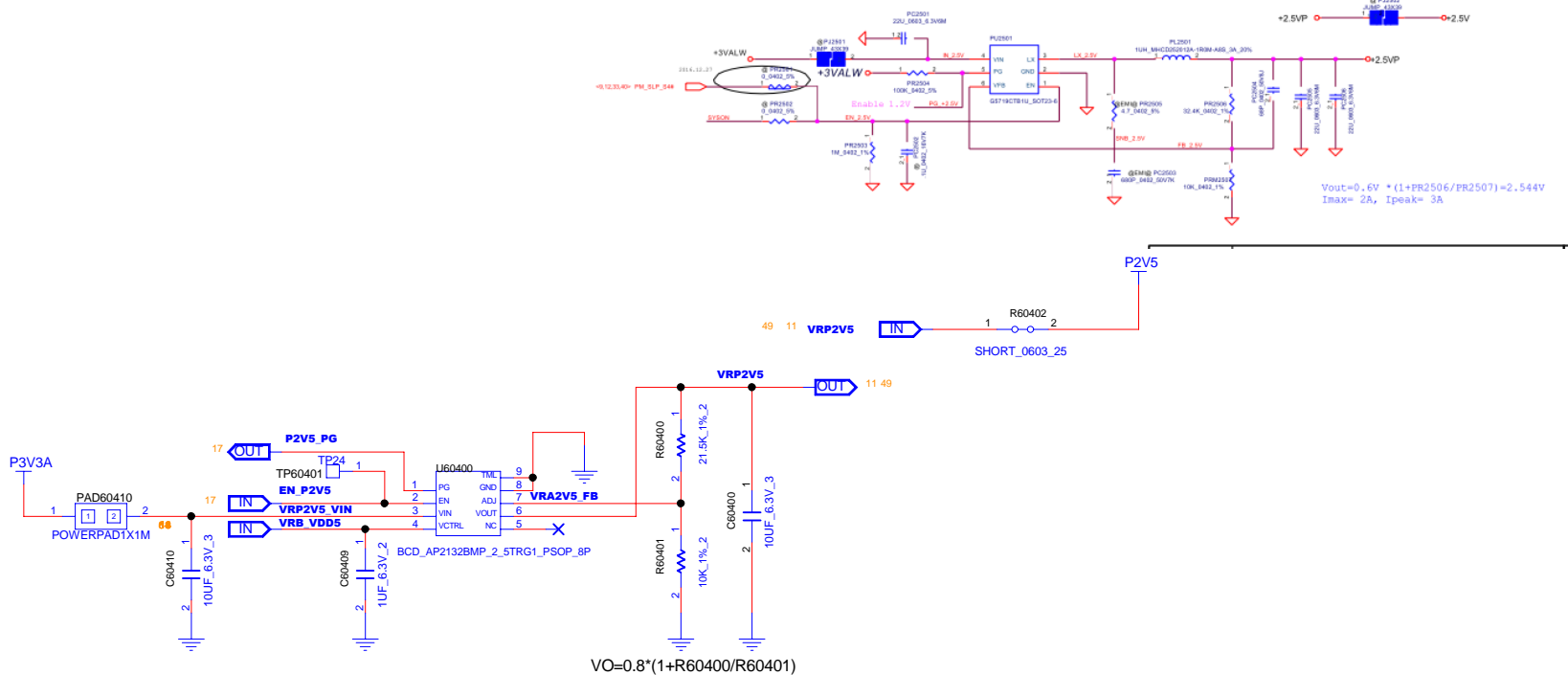




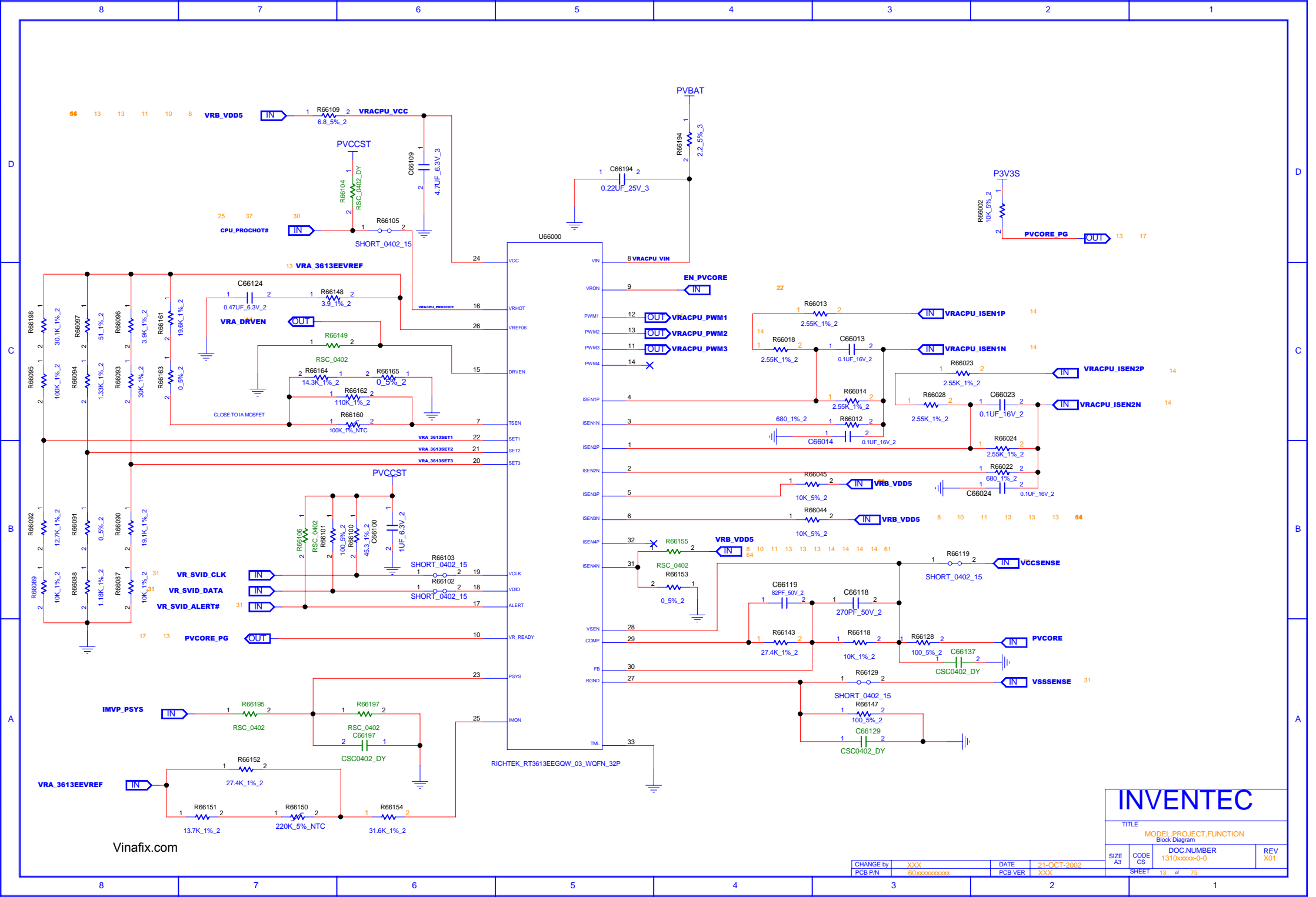












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MODEL PROJECT FUNCTION  
Block Diagram

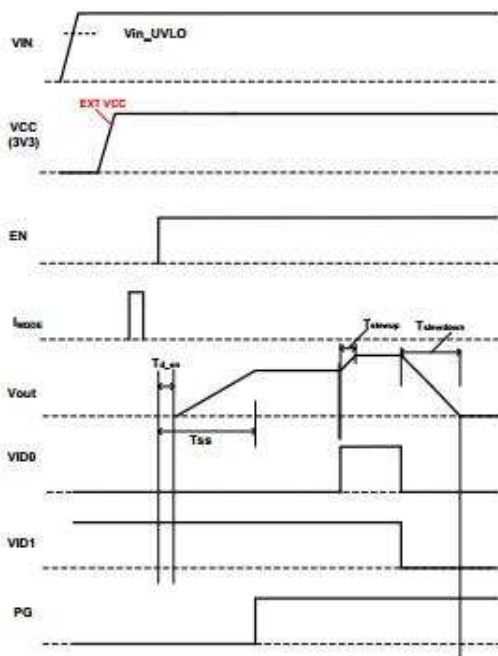
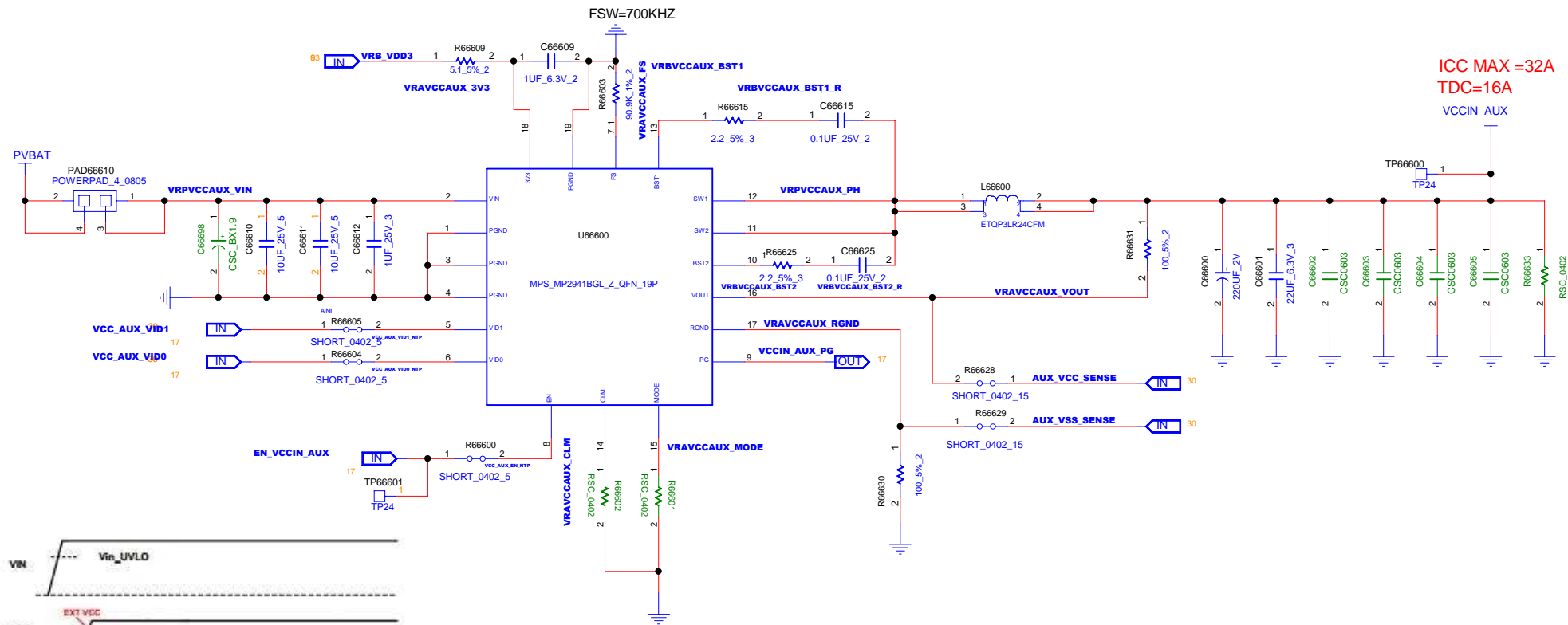
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CHANGE by XXX DATE 21-OCT-2002  
PCB P/N 60xxxxxxxxx PCB VER XXX

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**Figure 4—Start-up power sequence**  
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**Table 1—MODE Select**

State	Interleaving	VID Down	Resistor to GND
M1	N	Slew down	0
M2	Y	Slew down	90 K
M3	Y	Decay	150 K
M4	N	Decay	>230 K or float

**Table 2—FS Selection**

State	Fs	Resistor to GND
M1	500kHz	0
M2	700kHz	90 K
M3	1000kHz	150 K
M4	1200kHz	>230 K or float

**Table 3—VID control Bit logics**

VID1	VID0	VOUT(V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

**Table 4—CLM/Phase Selection**

State	CLM	Resistor to GND
M1	7A	0
M2	10A	90 K
M3	13A	150 K
M4	16A	>230 K or float

**INVENTEC**

TITLE  
MODEL PROJECT FUNCTION  
PVC001

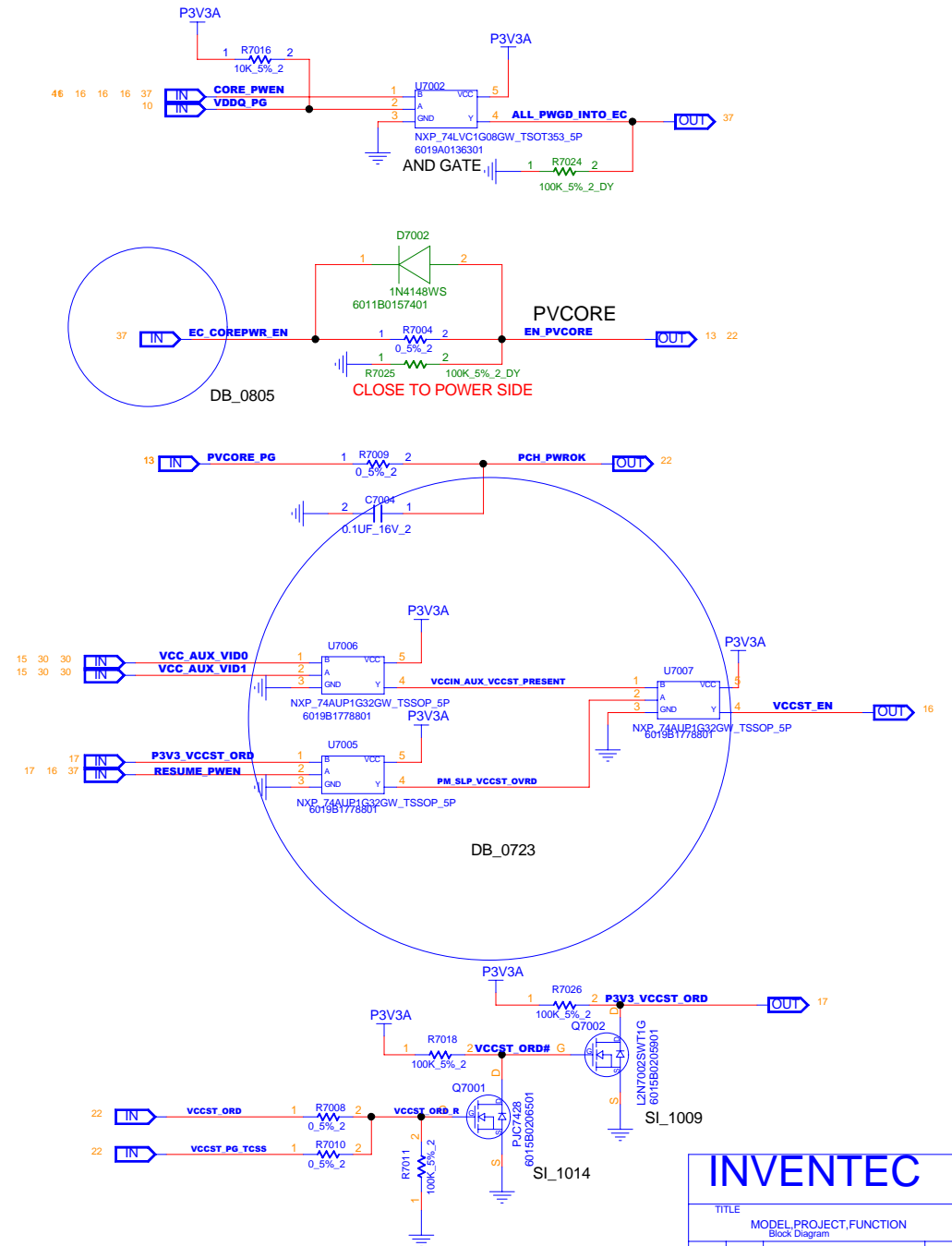
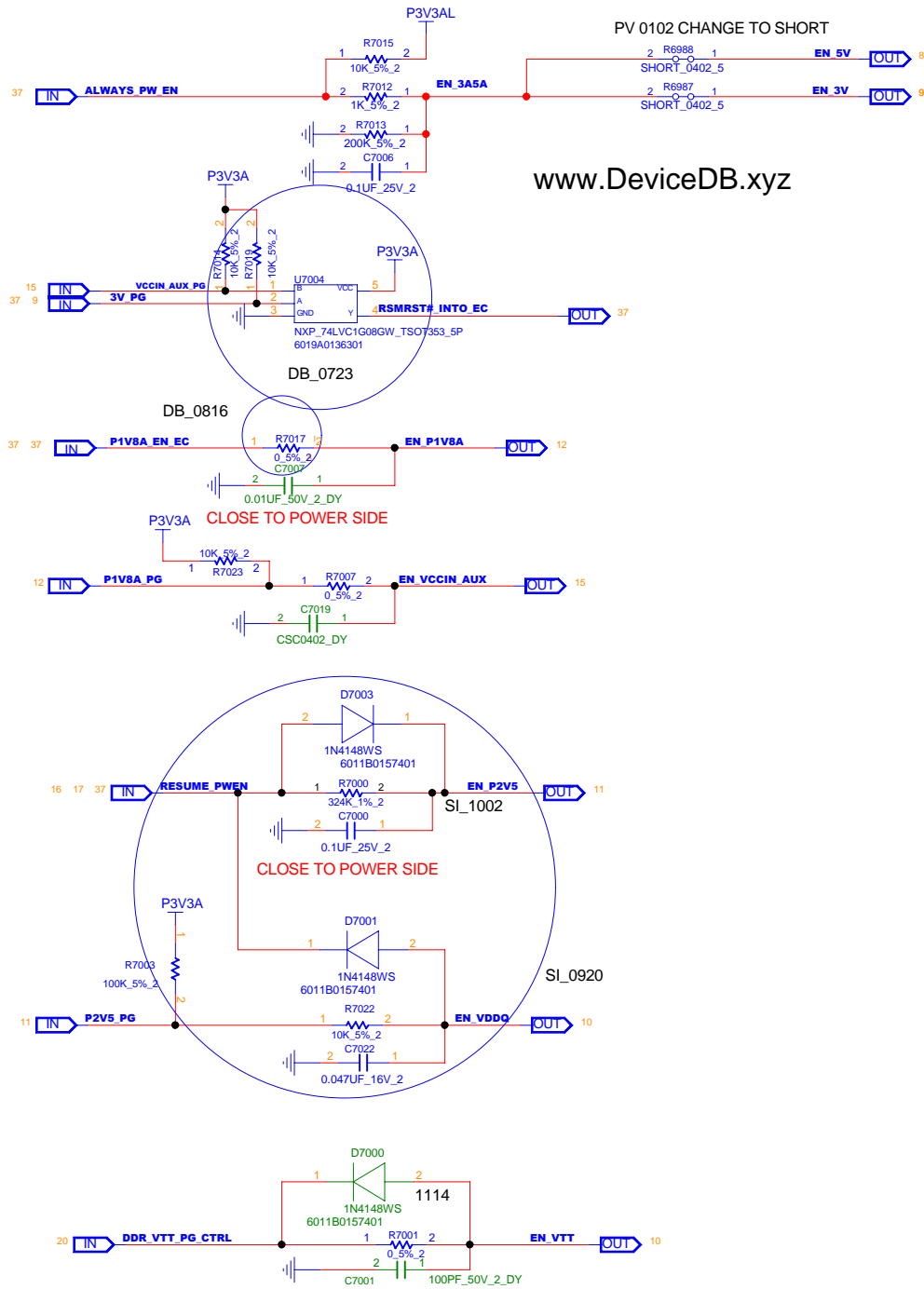
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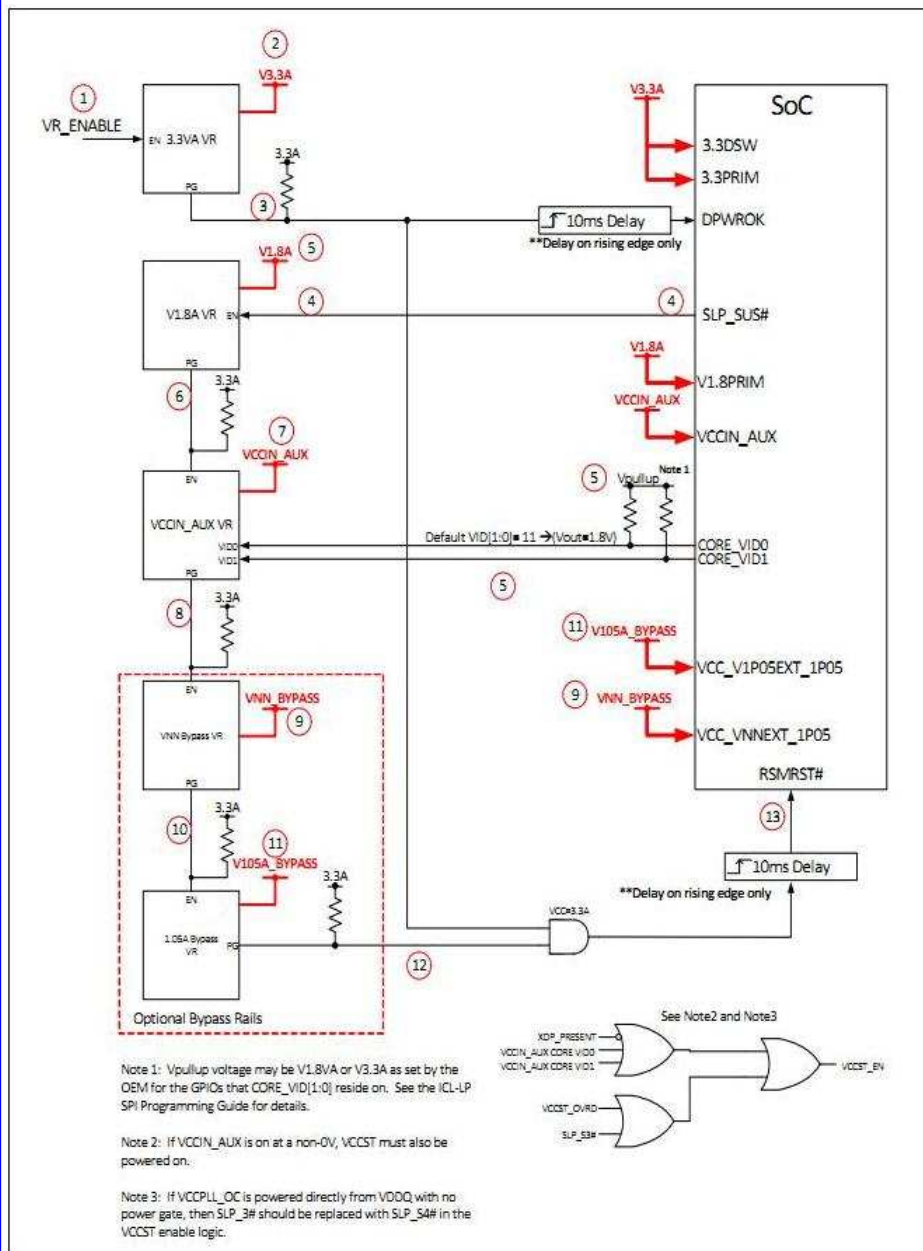
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Block Diagram

SIZE A3 CODE CS DOC NUMBER 1310xxxx-0-0 REV X01

CHANGE by XXX DATE PCB VER PCB REF 2002

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FIGURE 11-29. ICE LAKE NON-DSX SYSTEM ARCHITECTURE BLOCK DIAGRAM



## 11.12.4 Power States

Table 11-23. System with M3 State Supported

Rails	SKUs	S0/M0 <sup>3</sup>	C10 <sup>2</sup>	S0ix/M-off <sup>4</sup>	S3/M3	S3/M-off	S4 and S5/M3	S4 and S5/M-off	Deep S4/S5	G3 <sup>1</sup>
RTC Well	All	ON	ON	ON	ON	ON	ON	ON	ON	ON
3.3V_DSW	All	ON	ON	ON	ON	ON	ON	ON	ON	No Power
VBATA (VDC)	All	ON	ON	ON	ON	ON	ON	ON	ON	No Power
V5.0A	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
V3.3A	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
V1.8A	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
V1.0A	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VNN_BYPASS	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
V1.05_BYPASS	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
V3.3M <sup>5</sup>	All	ON	ON	OFF	ON <sup>10</sup>	OFF	ON <sup>10</sup>	OFF	OFF	No Power
V1.8M <sup>5</sup>	All	ON	ON	OFF	ON <sup>10</sup>	OFF	ON <sup>10</sup>	OFF	OFF	No Power
VDDQ	All	ON	ON	ON	ON	ON	OFF	OFF	OFF	No Power
V2.5U (VPP)	All	ON	ON	ON	ON	ON	OFF	OFF	OFF	No Power
VCCST <sup>12, 15</sup>	All	ON	ON	ON	ON <sup>13</sup>	ON <sup>13</sup>	OFF <sup>6</sup>	OFF <sup>6</sup>	OFF	No Power
VCCSTG	All	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	No Power
TCSS/AGSH	All	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	No Power
VCCPLL	All	ON	ON	ON	ON <sup>13</sup>	ON <sup>13</sup>	ON	ON	OFF	No Power
V3.3S	All	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	No Power
VCCPLL_OC <sup>12</sup>	All	ON	OFF <sup>11</sup>	OFF <sup>11</sup>	ON <sup>8, 13</sup>	ON <sup>8, 13</sup>	OFF	OFF	OFF	No Power
VCCIN	All	ON	ON	ON <sup>11</sup>	OFF	OFF	OFF	OFF	OFF	No Power
VCCIN_AUX	All	ON	ON	ON <sup>11</sup>	OFF <sup>14</sup>	OFF <sup>14</sup>	OFF <sup>14</sup>	OFF <sup>14</sup>	OFF	No Power

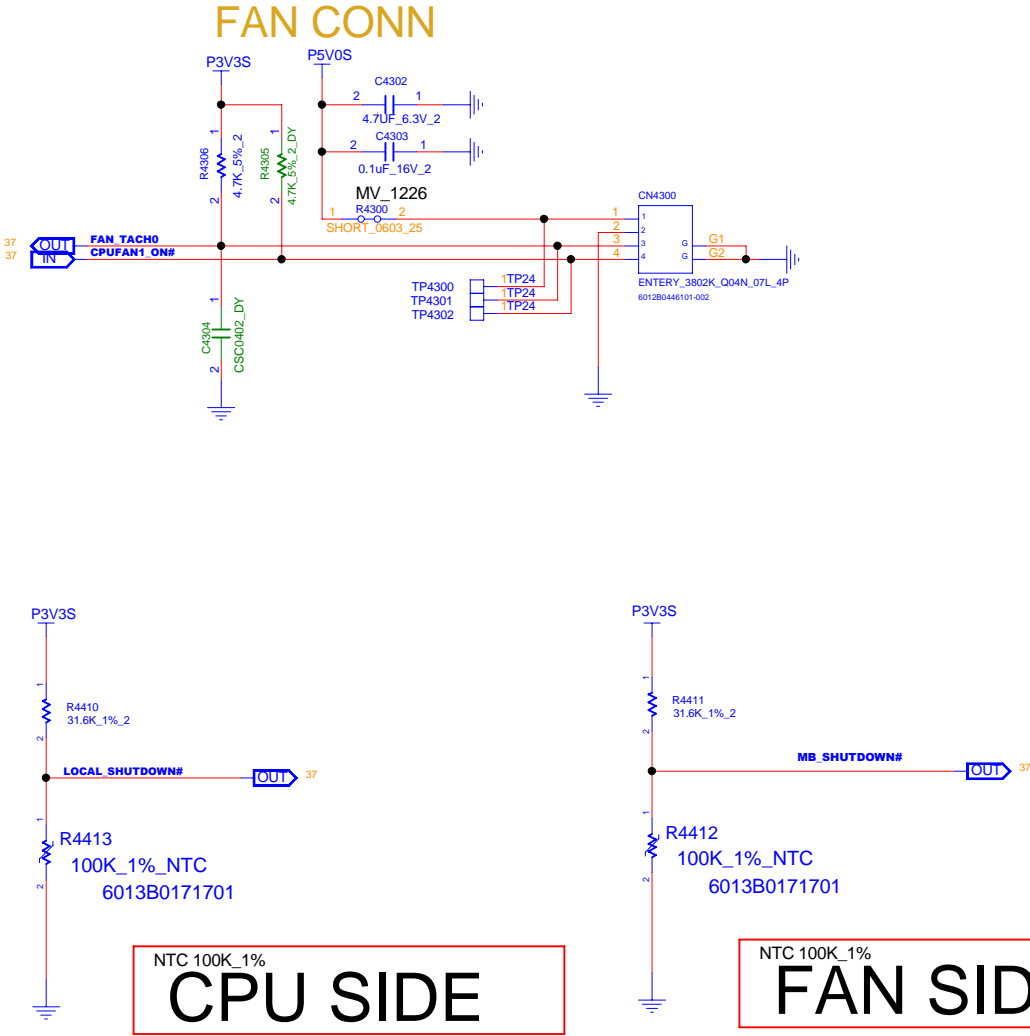
### Notes:

- The state of the system without RTC well powered can also be considered G3.
- VCCSTG, VCCPLL\_OC, TCSS, AGSH can be turned off when the processor is in C10.
- S0/M0 state includes all Package C-states from C0-C10.
- Assume SLP\_S0# and CPU\_C10\_GATE# have asserted from the PCH.
- V3.3M and V1.8M are platform rails used by external devices which ME operates during Sx/M3 states. These rails are not used directly by the CPU/PCH, and are not present on non-M3 supported systems.
- VCCST can remain powered during S4 and S5 power states for board cost optimization. VCCST may also remain powered in S4 and S5 for debug purposes. Refer to Chapter 13, "Platform Debug and Test Hooks" for more details.
- NA.
- VCCPLL\_OC is allowed to be turned off during S3, if it is not powered directly from VDDQ.
- Note that merging power rails may reduce power optimization opportunities on the platform.
- For no M3 support on external devices, V3.3M/V1.8M will be OFF in Sx/M3.
- This supply is expected to be 0V during states where SLP\_S0# is asserted. It may be left on during this condition, but the SoC will not achieve it is lowest power consumption. Specific power up latencies apply when exiting this state.
- VCCST should be "on" whenever VCCPLL\_OC is "on". VCCPLL\_OC must be "off" whenever VCCST is "off".
- For additional power savings in S3, Refer Section 11.12.5.
- VCCIN\_AUX may be ON in these power states if required by the SoC.
- VCCST must be ON if VCCIN\_AUX is ON, this applies to all Sx power states.

# FAN & THERMAL

FOR BIG CORE USE

VER.04\_20171011



U4555

U4555

INTEL\_J52741\_BGA\_1526P

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INTEL\_J52741\_BGA\_1526P

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INTEL\_J52741\_BGA\_1526P

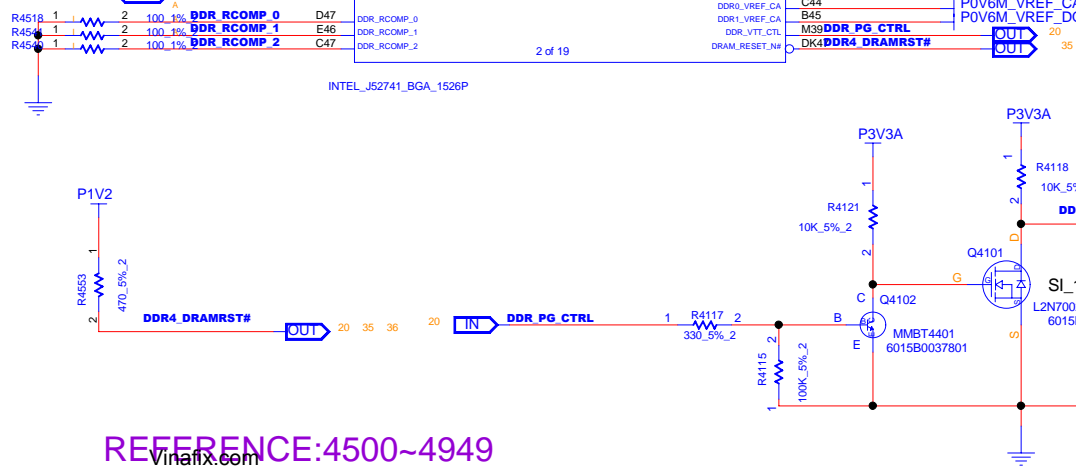
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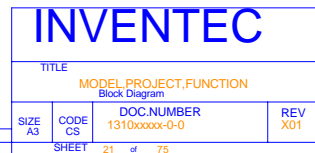
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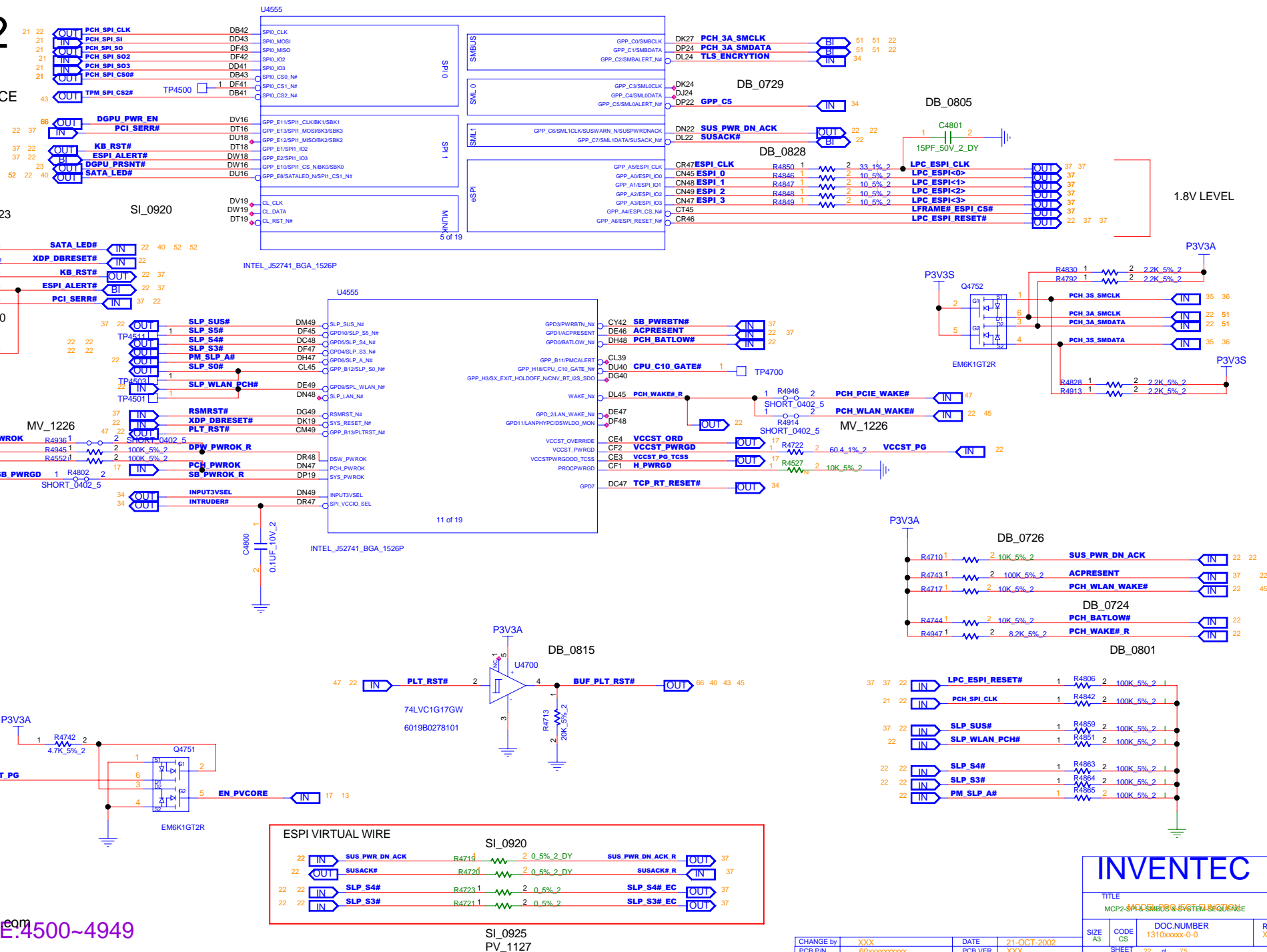
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PCB P/N 60xxxxxxxxx PCB VER XXX

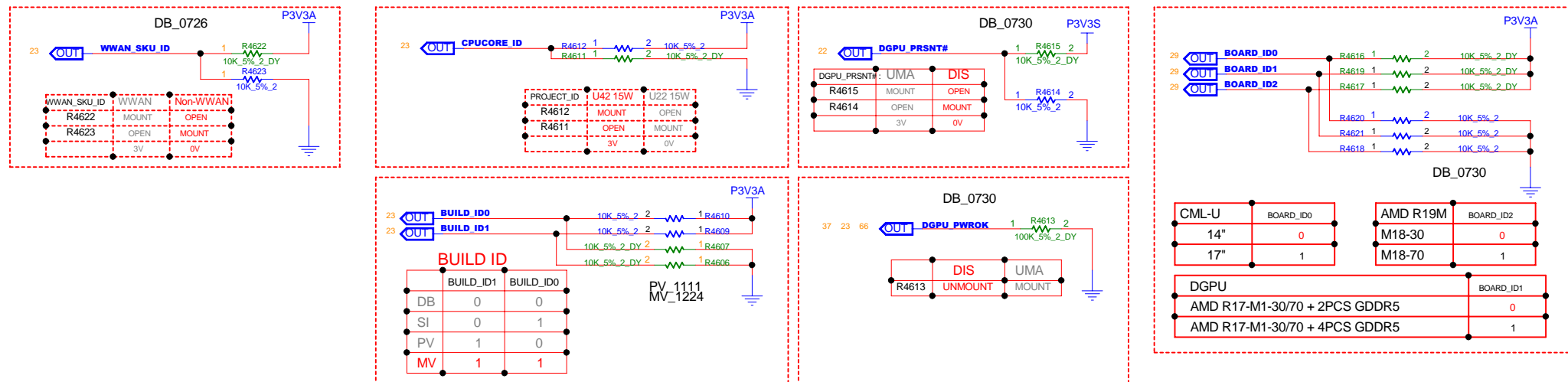
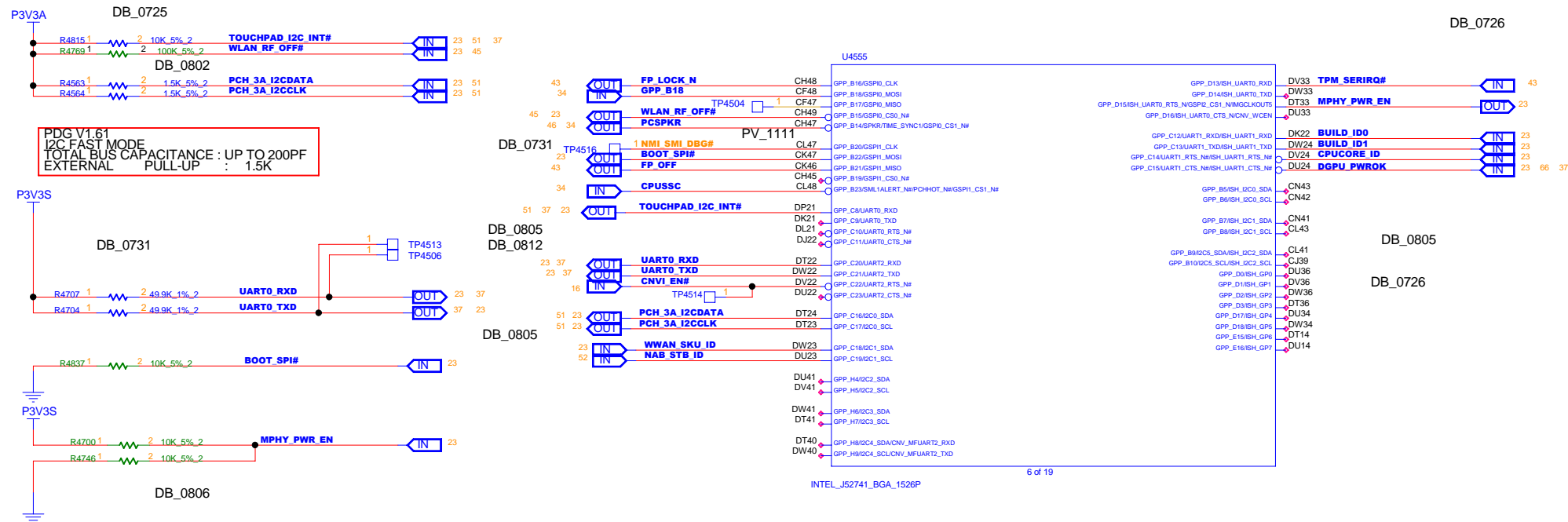
## A





SPI  
SMBUS  
SYSTEM SEQUENCE

# CPU-3 GPIO



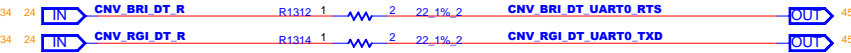
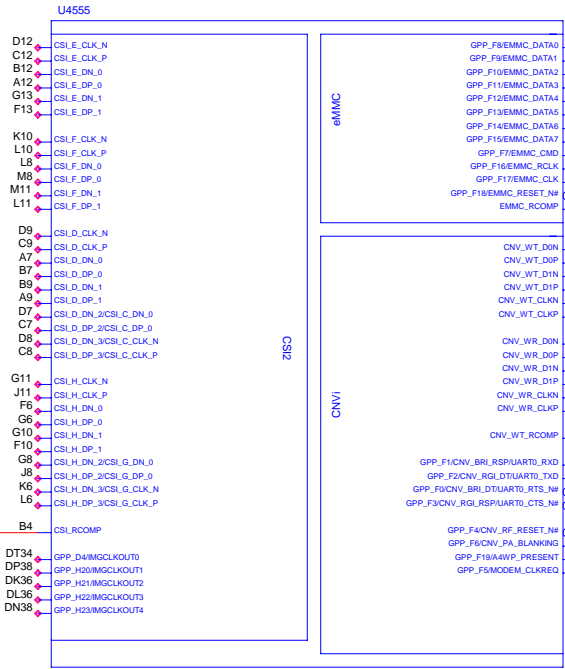
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# CPU-4 GPIO, CNVI

DB\_0726

DB\_0815-2

DB\_0814



REFERENCE:4500~4949  
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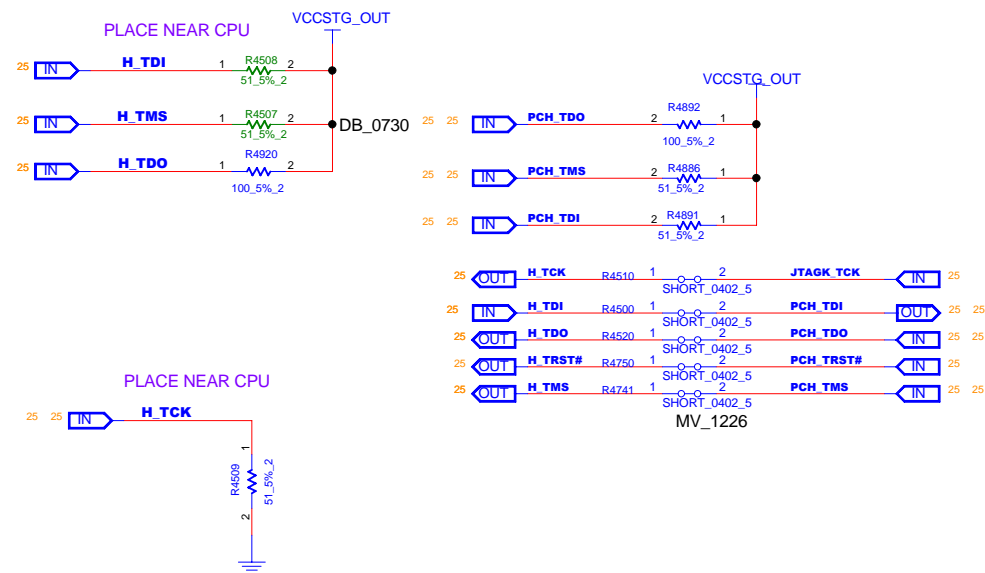
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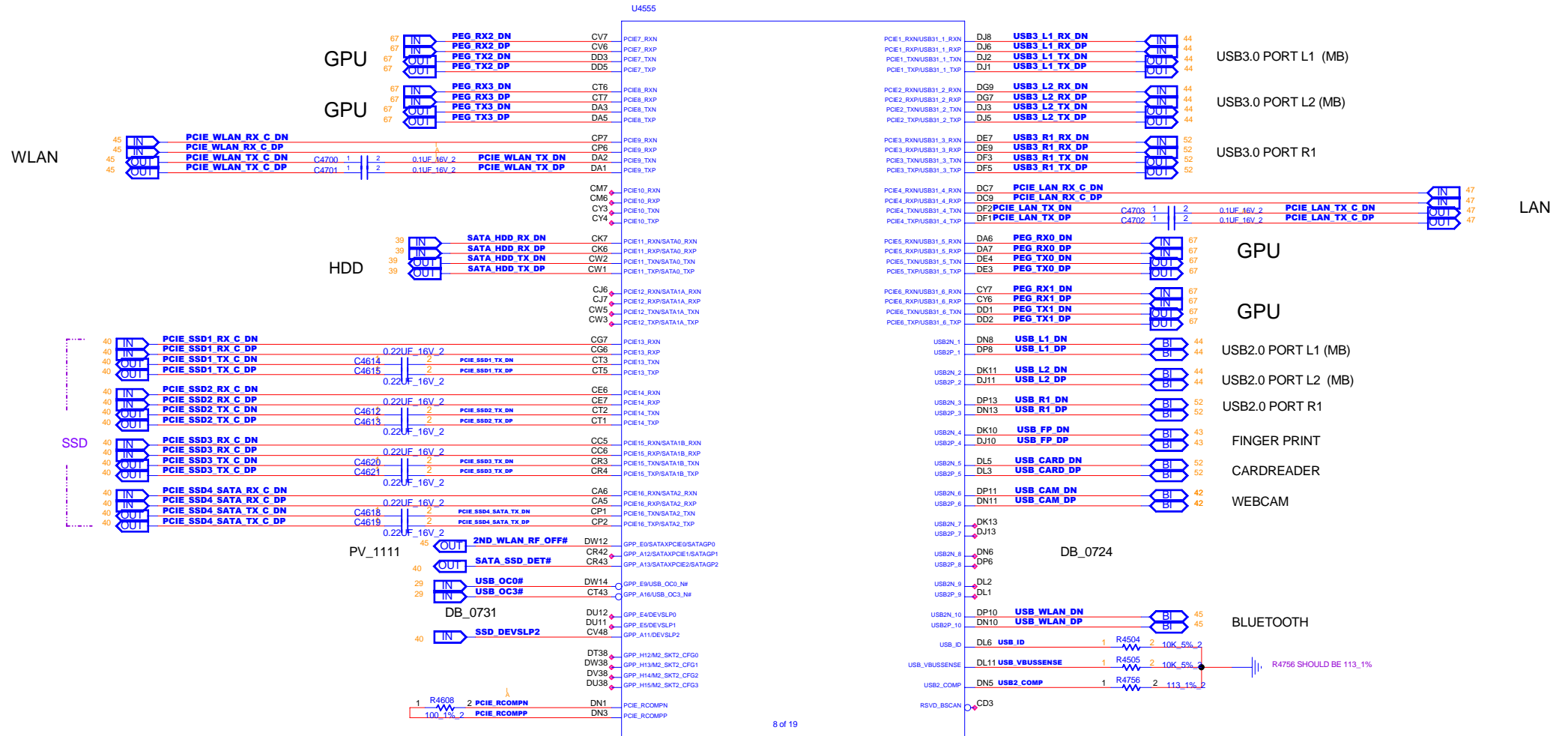


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INVENTEC			
TITLE			
MODEL: PROTEST, FUNCTION			
SIZE A3	CODE CS	DOC. NUMBER 1310xxxx-0-0	REV X01
SHEET 25 of 75			

## CPU-6 PCIE, USB



INTEL\_J52741\_BGA\_1526P

CHIPSSET SKU	Max Number of USB 2.0 Ports	USB 2.0 Port # 1	USB 2.0 Port # 2	USB 2.0 Port # 3	USB 2.0 Port # 4	USB 2.0 Port # 5	USB 2.0 Port # 6	USB 2.0 Port # 7	USB 2.0 Port # 8	USB 2.0 Port # 9	USB 2.0 Port # 10	Integrated Wireless AC
Premium-Y	6											
Premium-U	10											

Port Disabled

Port Enabled

Port Enabled for Integrated Wireless-AC only

DB\_0726

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REFERENCE:4700~4949

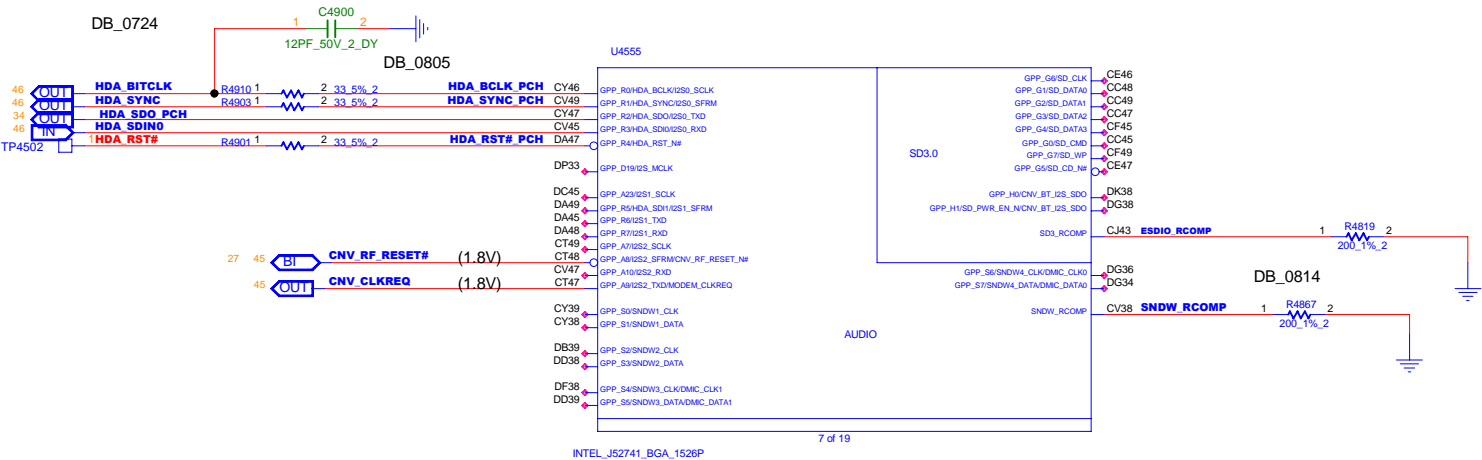
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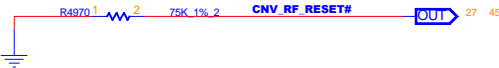
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PCB P/N	60xxxxxxxxxx	PCB VER	XXX

# CPU-7 RTC, AUDIO, SATA



LAYOUT NOTE: PLACE R4808 NEAR PCH  
LAYOUT NOTE: JTAG\_TMS TERMINATIONS NEED TO BE PLACED NEAR PCH  
LAYOUT NOTE: JTAG\_TDI TERMINATIONS NEED TO BE PLACED NEAR PCH  
LAYOUT NOTE: JTAG\_TDO TERMINATIONS NEED TO BE PLACED NEAR XDP



REFERENCE:4500~4949  
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INVENTEC

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MODEL PROJECT FUNCTION  
MC77-RTC & AUDIO & SATA

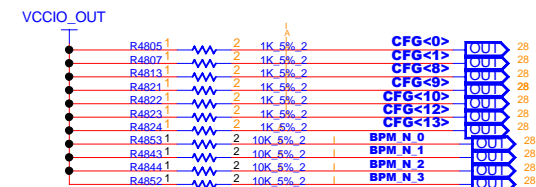
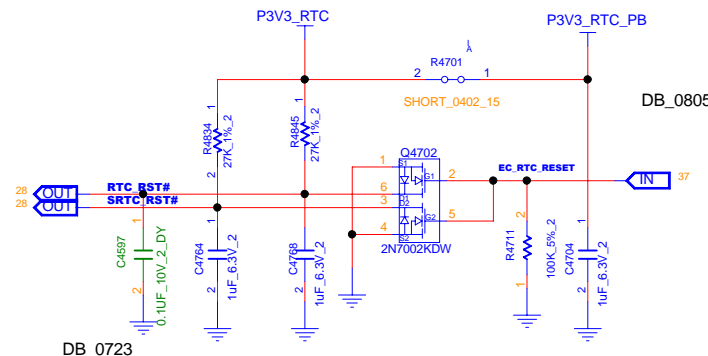
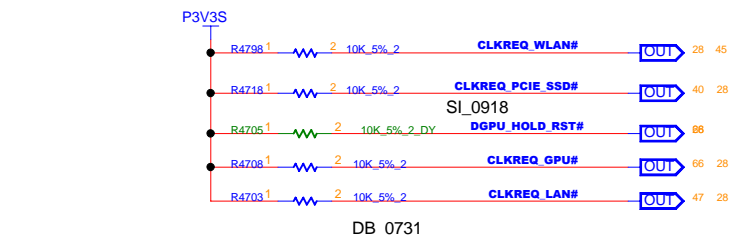
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REV X01

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PCB P/N 60xxxxxxxxx  
DATE 21-OCT-2002  
PCB VER XXX

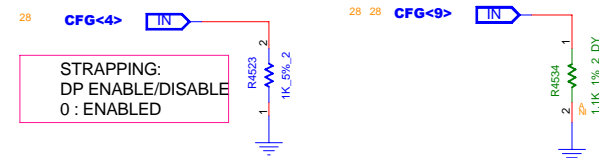
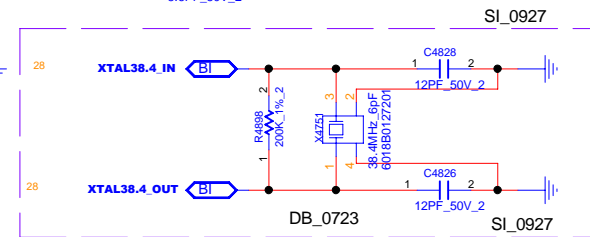
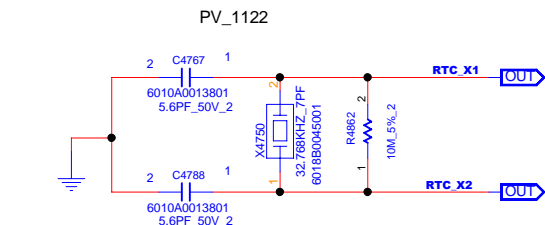
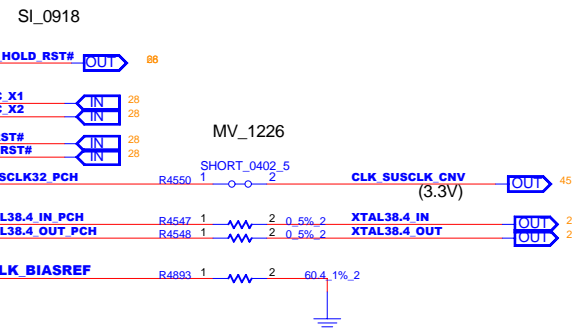
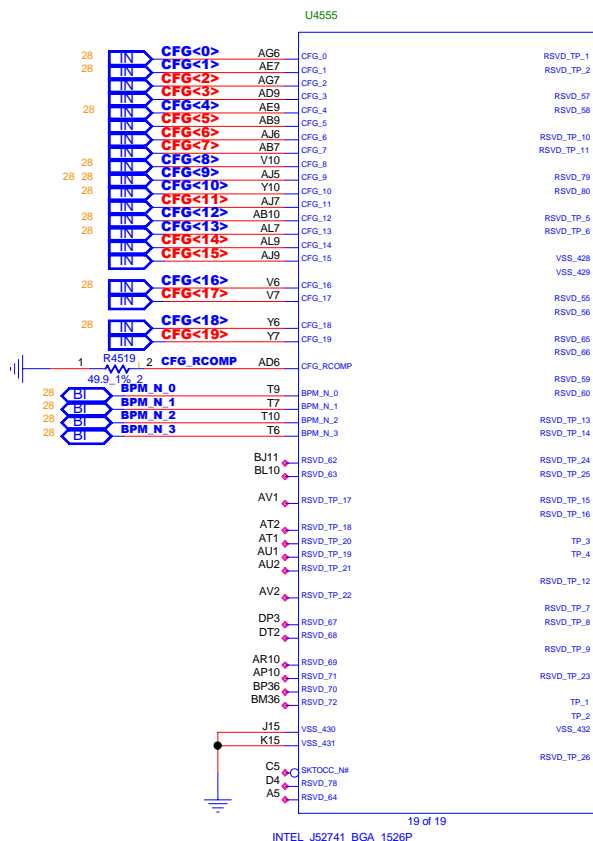
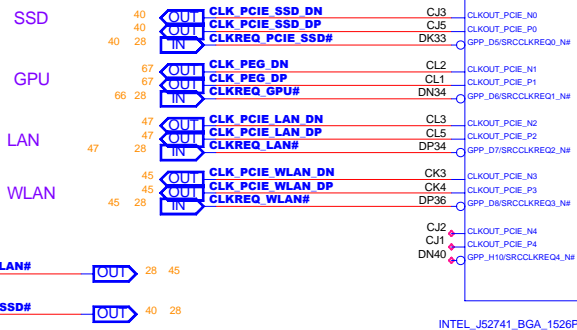
# CPU-8

CLOCK, RESERVED

## RTC



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REFERENCE:4500~4949



STRAPPING:  
DP ENABLE/DISABLE  
0 : ENABLED

## INVENTEC

TITLE  
MODEL PROJECT FUNCTION  
MCPE-CLOCK & RESERVED

SIZE A3 CODE CS DOC NUMBER 1310xxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002  
PCB P/N 60xxxxxxx PCB VER XXXX SHEET 28 of 75

D

C

B

A

DB\_0812

## INVENTEC

TITLE	MODEL PROJECT FUNCTION
	MCP4-GPIO & DP

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0
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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

REFERENCE:4500~4949



SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0
SHEET		30 of 75

CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	1310xxxxx-0-0	X01
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX	SHEET	30	of 75	

## D



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC			
TITLE MODIFIED PROJECT FUNCTION			
SIZE A3	CODE CS	DOC. NUMBER 1310xxxx-0-0	REV X01
SHEET 31 of 75			

# CPU-12 POWER2

ROUTE VCCSENSE WITH 27.4OHM IMPEDANCE

PLACE IN BACK SIDE

PLACE IN BACK SIDE

PLACE IN TOP SIDE

PLEASE PLACE CAPS CLOSE TO CPU

Table 11-8. Differences between Power Maps

Volume	Premium
VccSTG gated by SLP_S3#	VccSTG gated by {CPU_C10_GATE#}
VccPLL_OC is supplied directly from VDDQ	VccPLL_OC is supplied from VDDQ through a load switch
VCC1P8A on the CPU is supplied directly by V1.8A	VCC1P8A is supplied from V1.8A and gated by CPU_C10_GATE #
VCC_VNNEXT_1P05 is not used	VCC_VNNEXT_1P05 is supplied by small dedicated VNN VR to bypass PCH FIVR during light load
VCC_V1P05EXT_1P05 is not used	VCC_V1P05EXT_1P05 is supplied by small dedicated V1.05A VR to bypass PCH FIVR during light load

REFERENCE:4500~4949

INVENTEC

TITLE  
MONITOR POWER FUNCTION

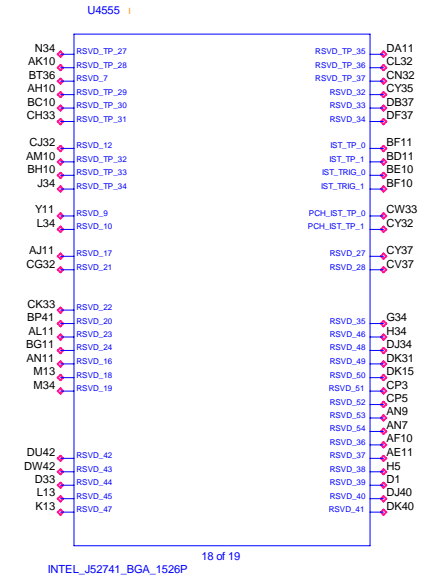
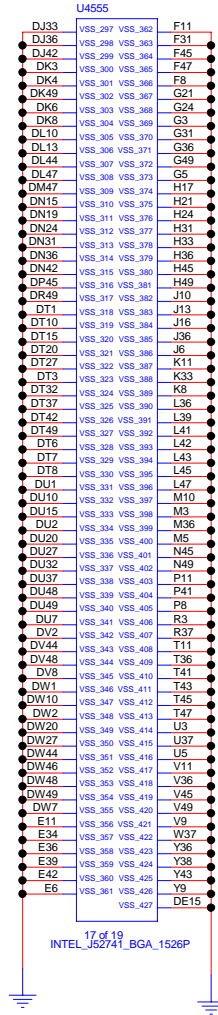
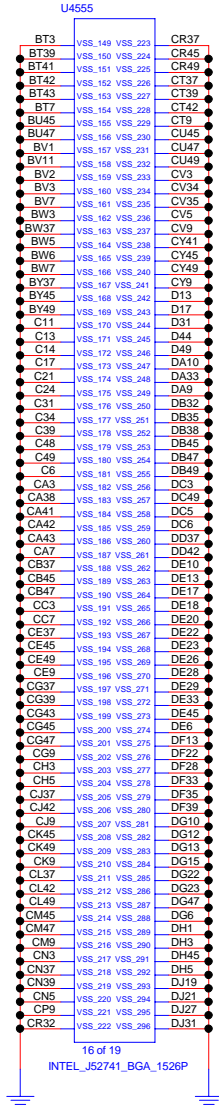
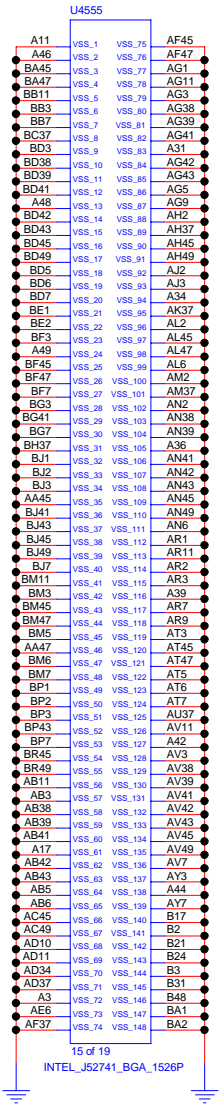
SIZE A3 CODE CS DOC NUMBER 1310xxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002  
PCB P/N 60xxxxxxxxx PCB VER XXX

SHEET 32 of 75



CPU-13 GND



REFERENCE:4500~4949

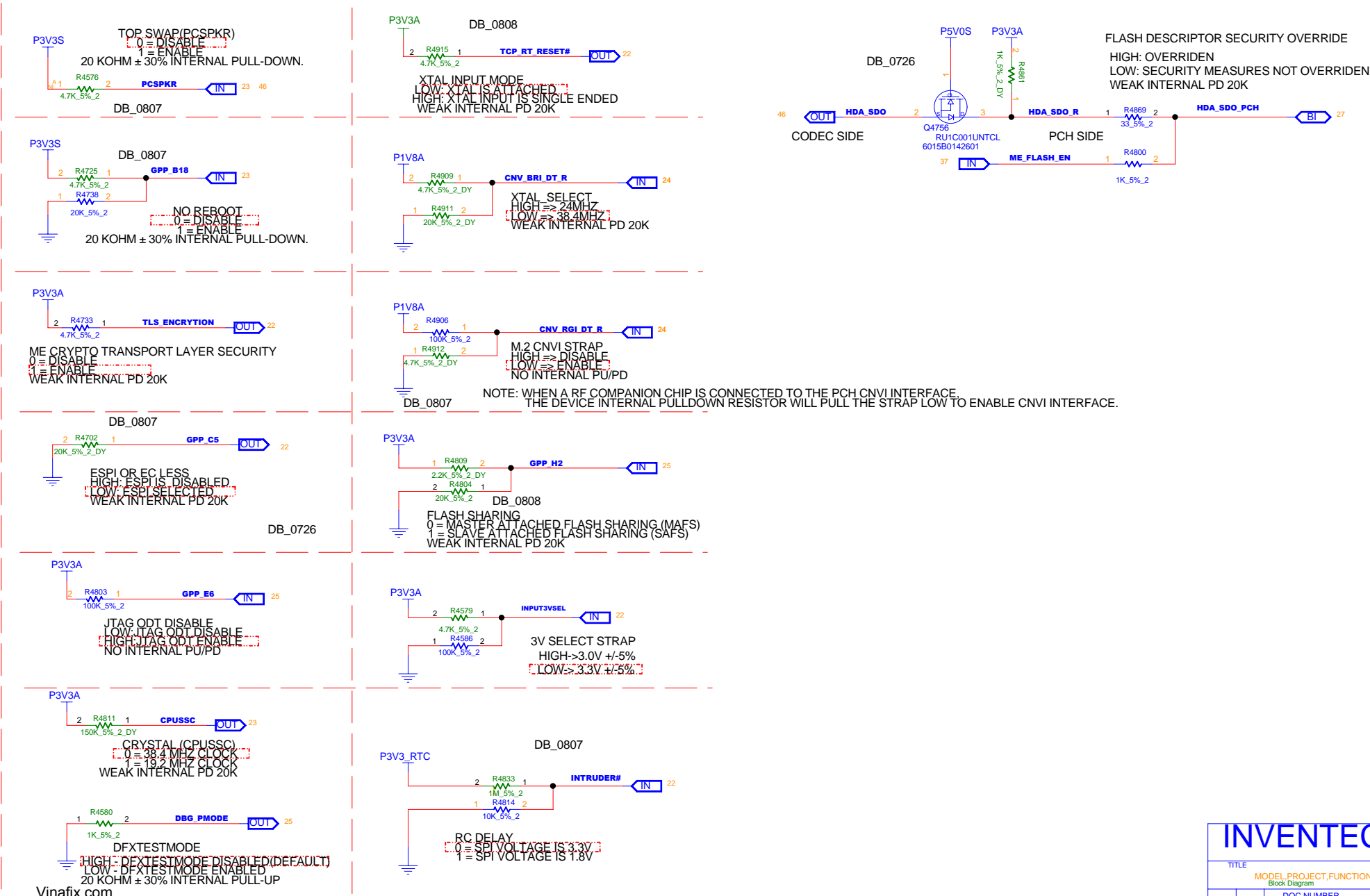
Vinafix.com

INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET 33 of 75			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

# CPU-14 STRAP



Vinafix.com

## INVENTEC

TITLE  
MODEL PROJECT FUNCTION  
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
------------	------------	----------------------------	------------

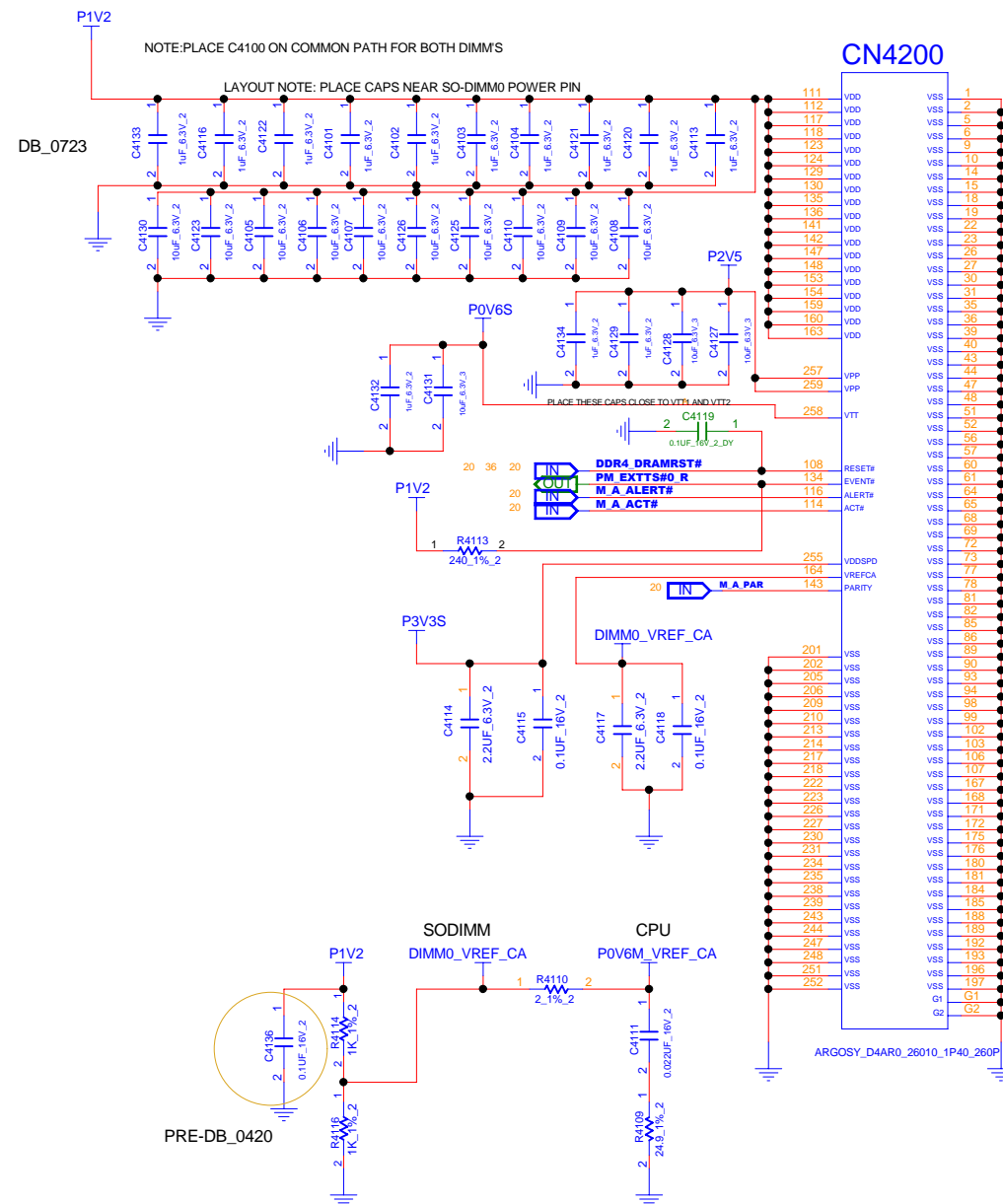
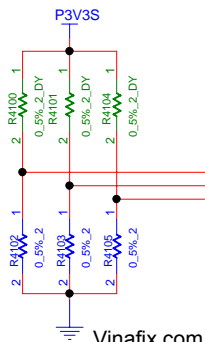
SHEET 34 of 75

CHANGE by PCB P/N	XXX 60xxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
----------------------	---------------------	-----------------	--------------------

CHA  
H=4



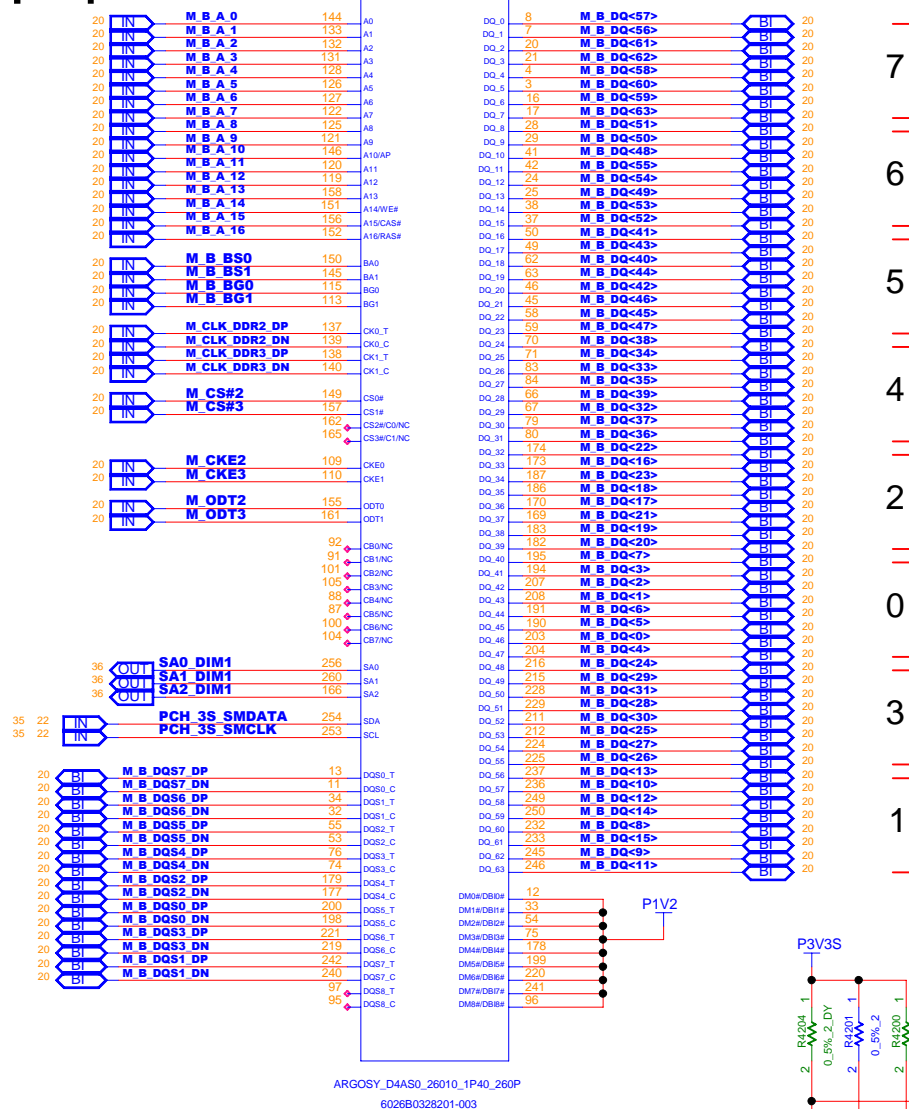
```
SPD ADDRESS FOR CHANNEL-0
WRITE ADDRESS:0XA0
RED ADDRESS :0XA1
SA0=0,SA1=0,SA2=0
DDR4 FOR OPERATING SPEED:1867 MT/S
STRETCH GOAL IS 2133 MT/S
EVENT_N: INDICATES THERMAL EVENT ON DIMM.
EVENT_N:ON ECC DIMM:KEEP A PULL UP IF NO PIN IN PCH
```



INVENTEC

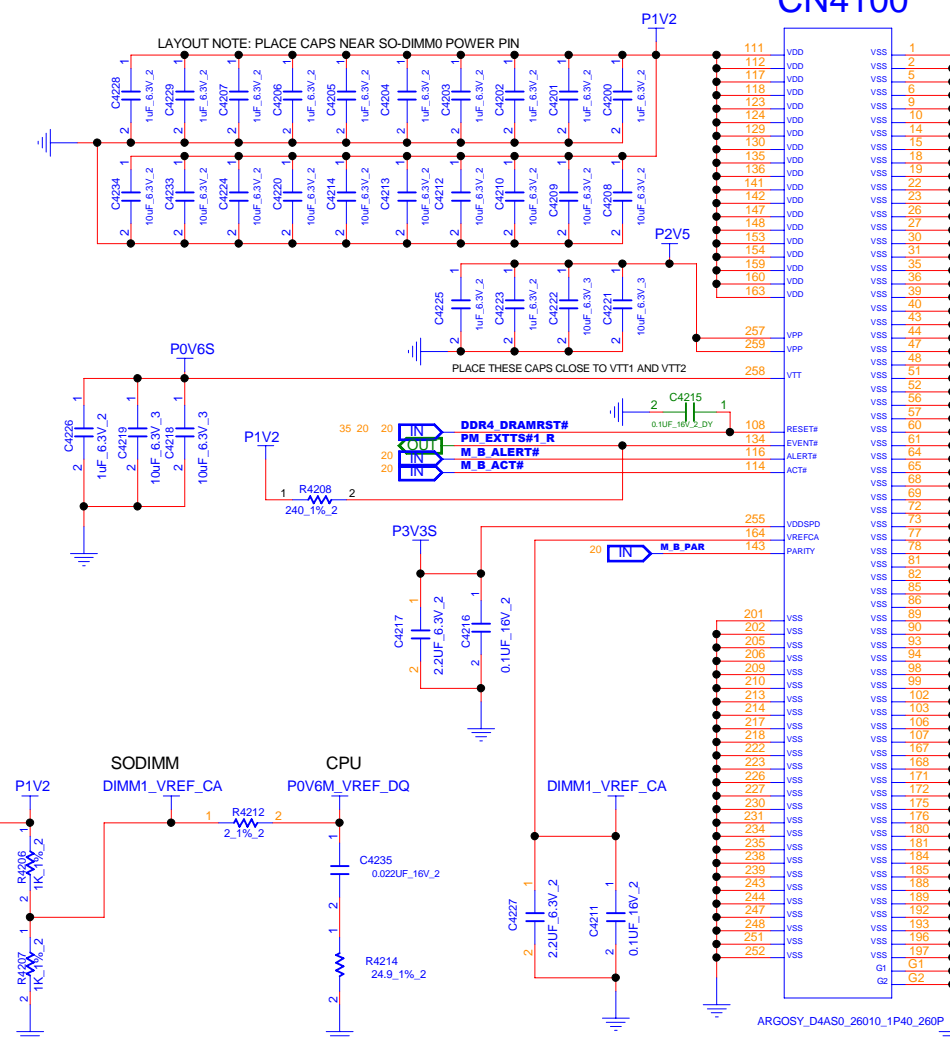
TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET		35 of 75	

CN4100



Vinafix.com

CN4100



EVENT\_N: INDICATES THERMAL EVENT ON DIMM.  
EVENT\_N:ON ECC DIMM:KEEP A PULL UP IF NO PIN IN PCH

INVENTEC

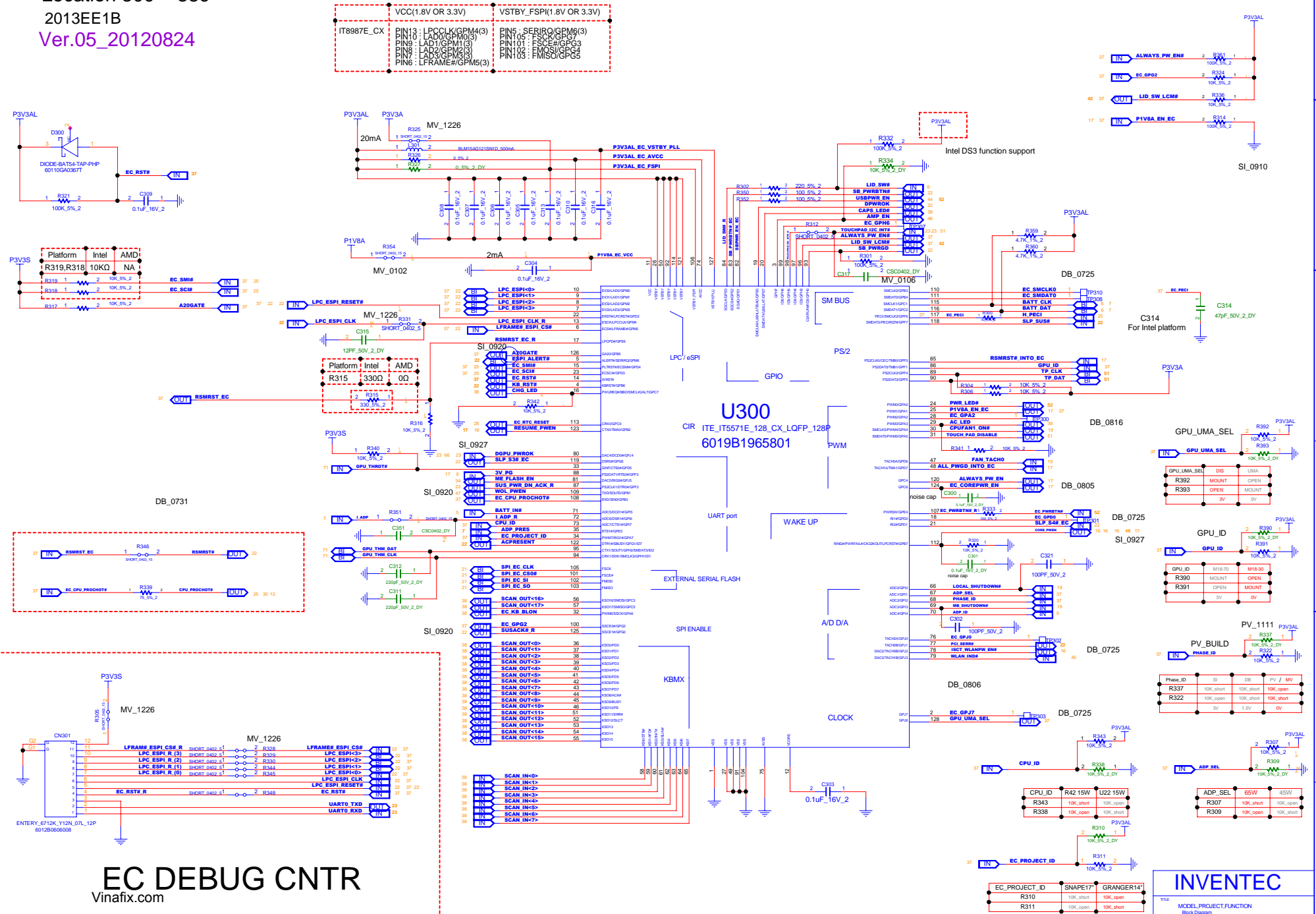
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET		36 of 75	

EC

Location 300 ~ 389

2013EE1B

Ver.05\_20120824



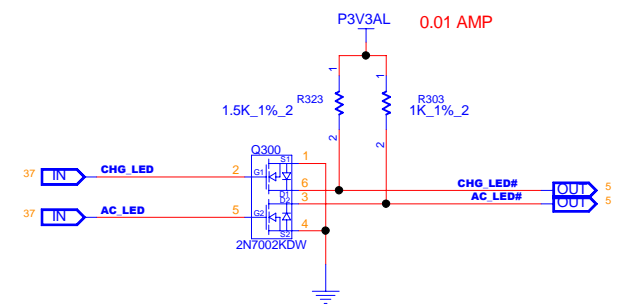
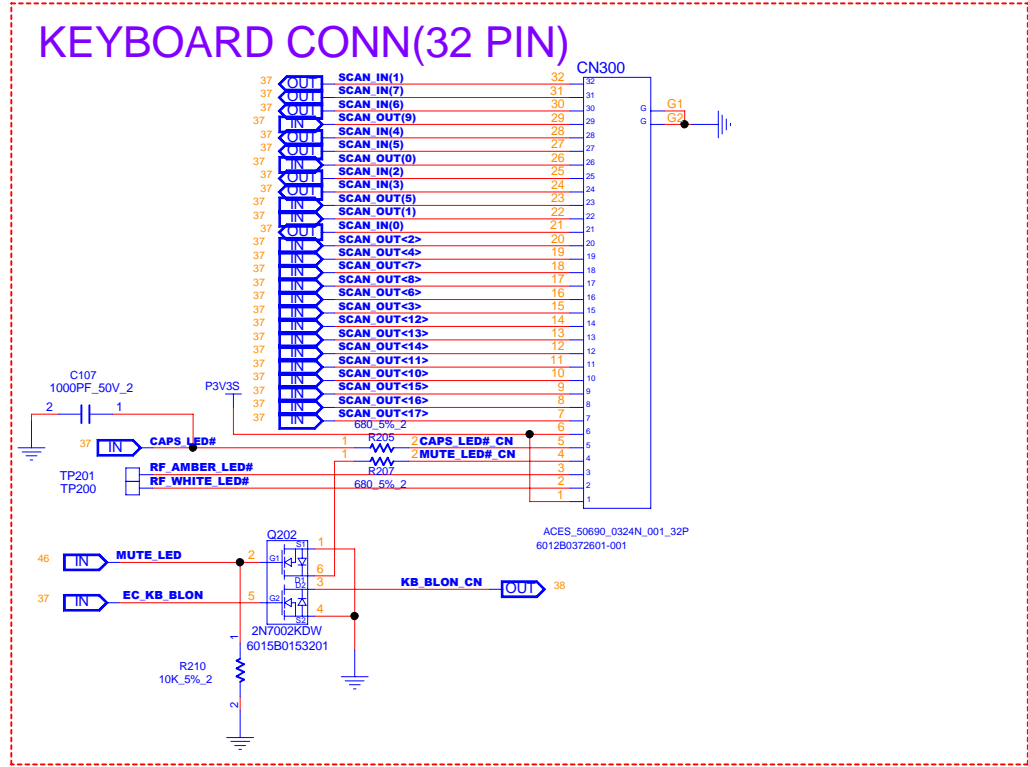
EC DEBU CNTR  
Vinafix.com

INVENTEC

# KEYBOARD CONNECTOR

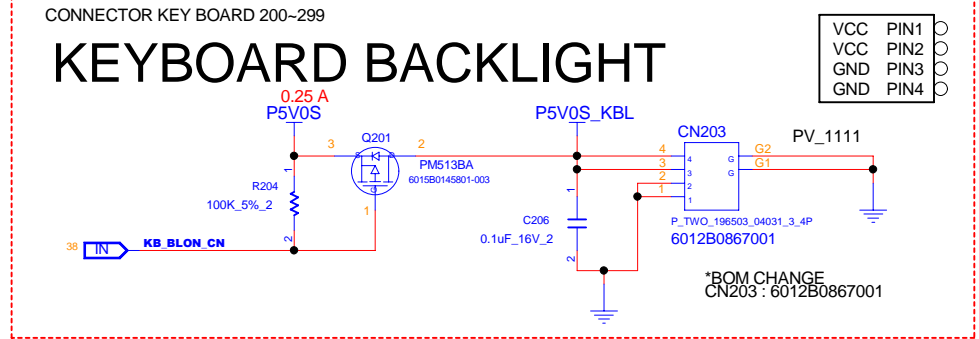
VER.07\_20171110

## KEYBOARD CONN(32 PIN)



CONNECTOR KEY BOARD 200-299

## KEYBOARD BACKLIGHT



Vinafix.com

INVENTEC

TITLE

MODEL PROJECT FUNCTION

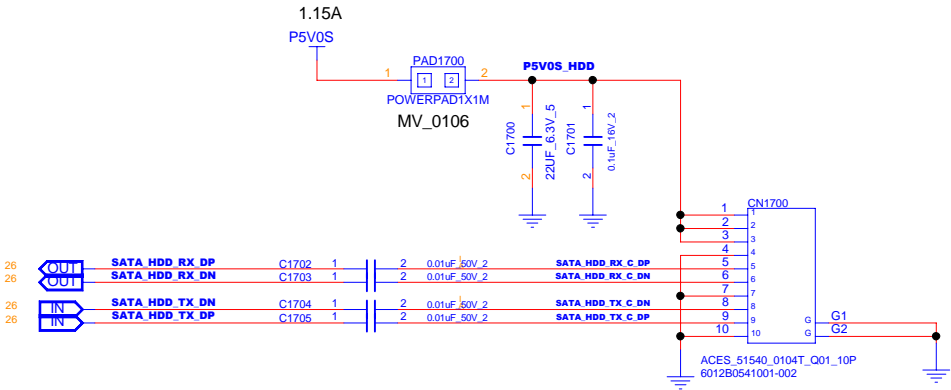
SIZE A3 CODE CS DOC NUMBER 1310xxxx-0-0 REV X01

CHANGE by XENG> DATE 21-OCT-2002 PCB VER XVER>

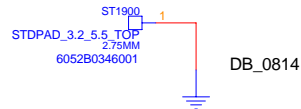
SHEET 38 of 75

# SATA HDD CABLE CONN on MB

VER.01\_20170918



VER.03\_20171004



CHANGE by	XEN>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XVER>

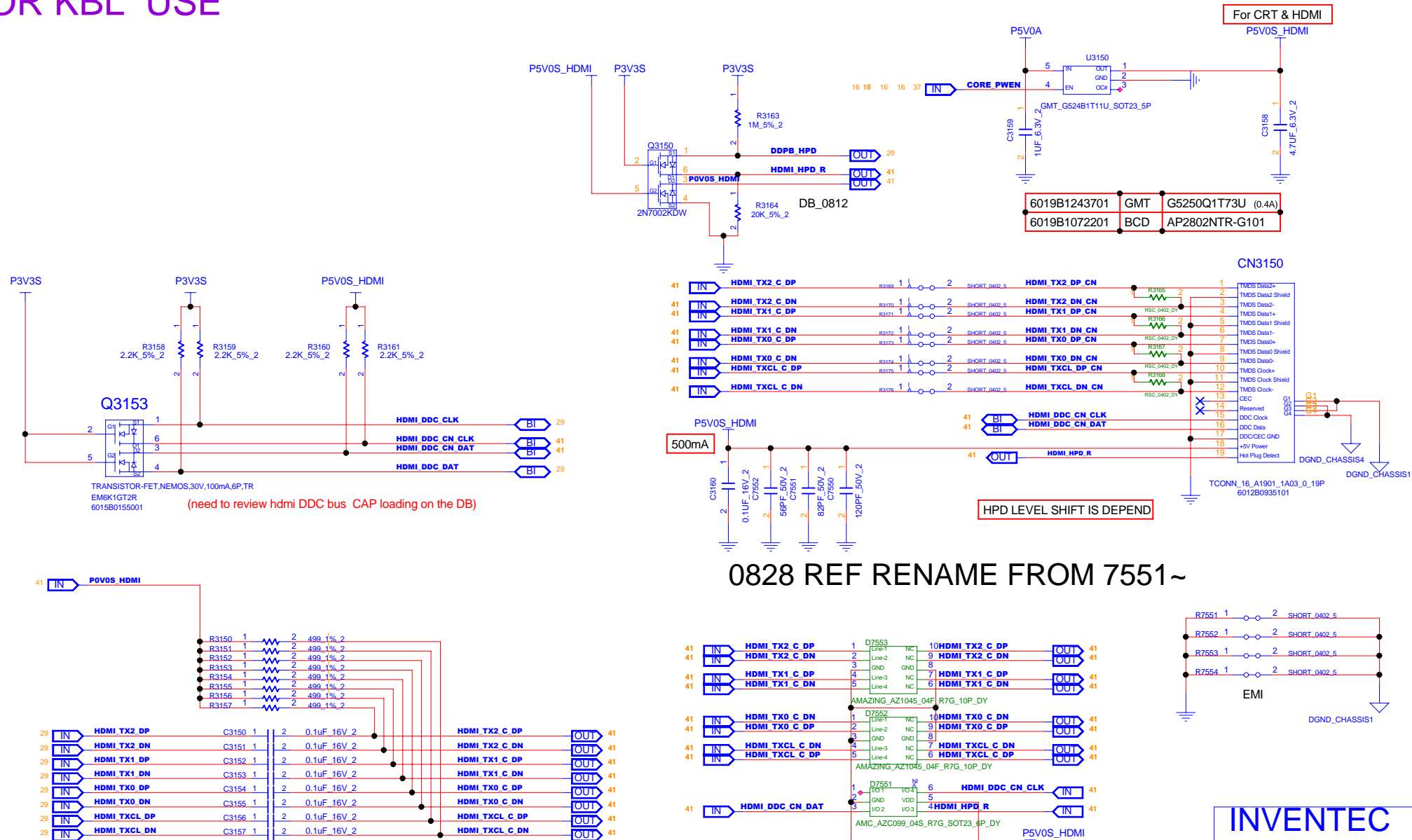


# HDMI

Location 3150 ~ 3199

VER.08\_20171115-2

## FOR KBL USE

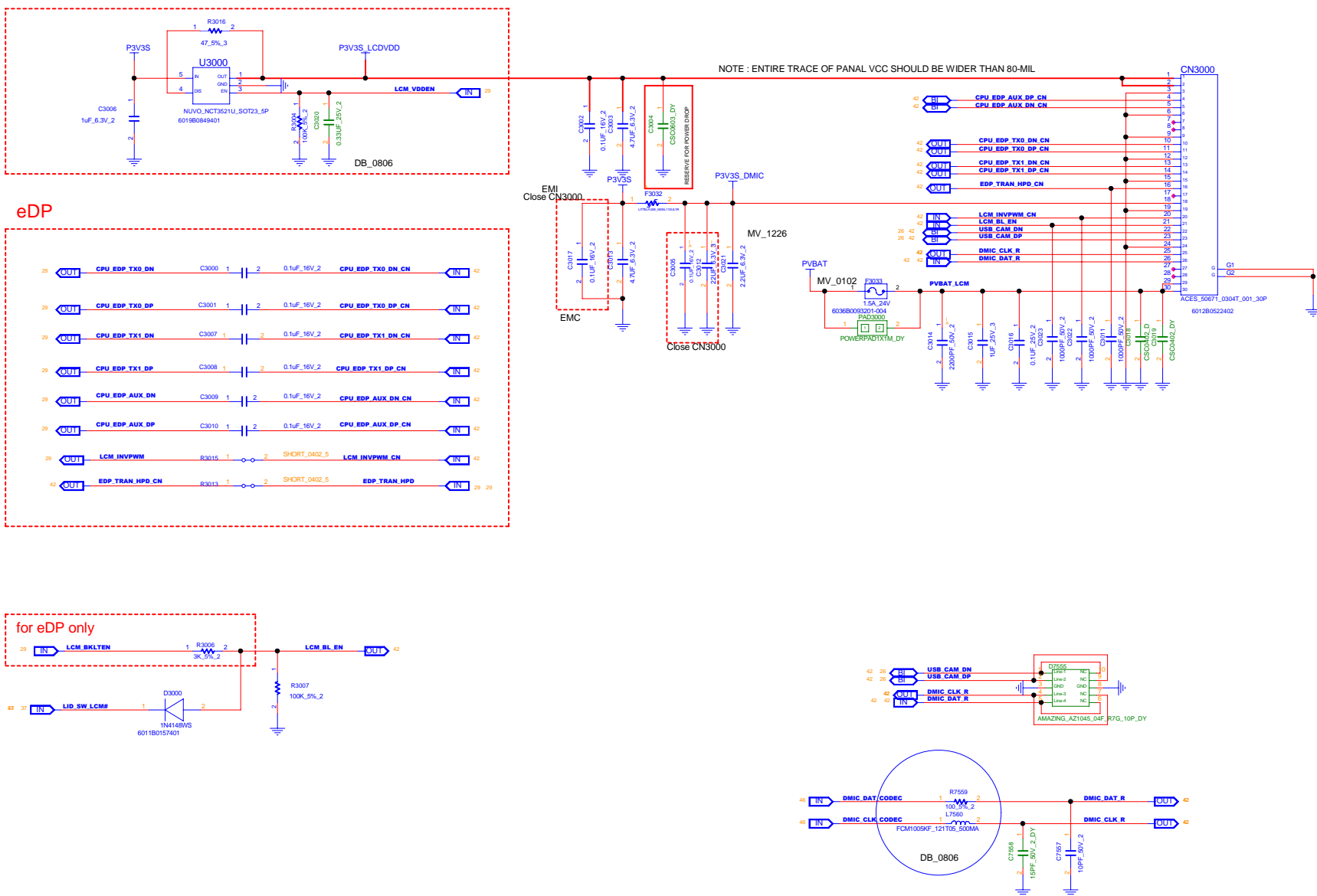


0828 REF RENAME FROM 7551~

INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
HDMI CORN			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET		41 of 75	

CHANGE by	XENG	DATE	21-OCT-2002
PCB P/N	60xxxxxxx	PCB VER	XVER

LCM : eDP  
LOCATION 3000 ~ 3049

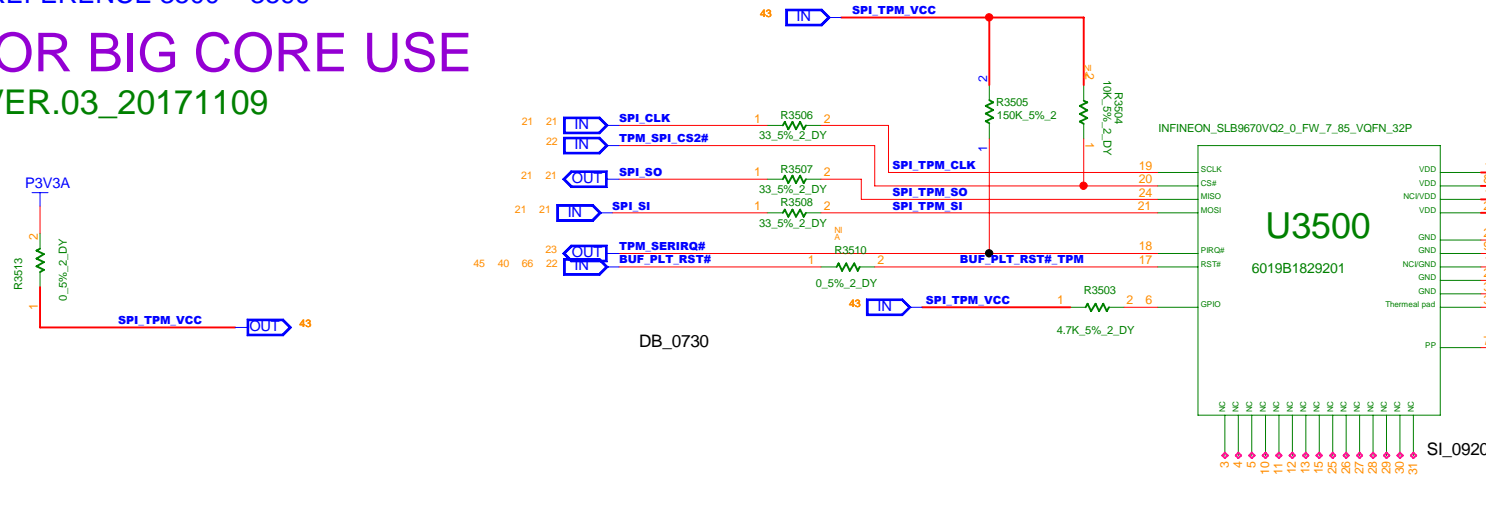


# TPM2.0

REFERENCE 3500 ~ 3599

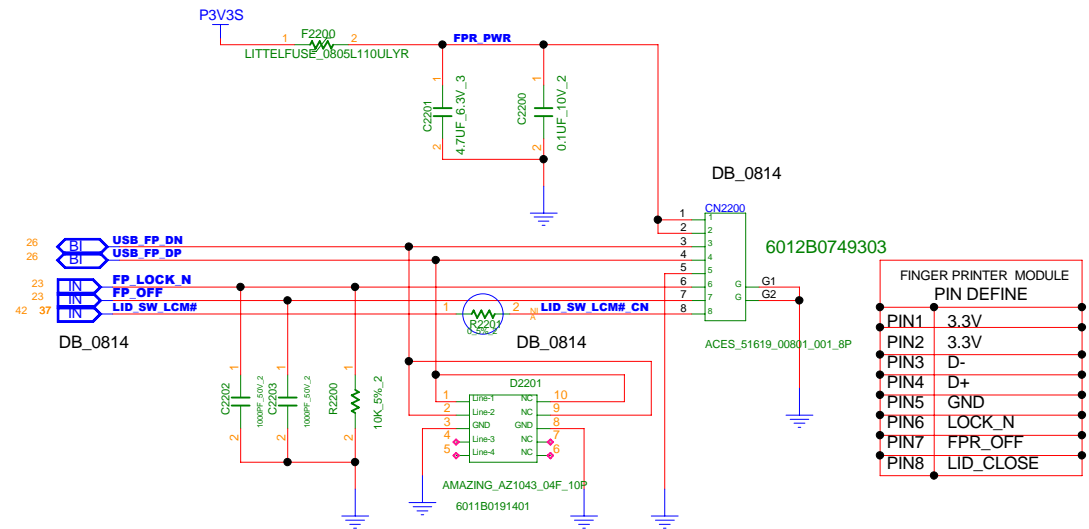
## FOR BIG CORE USE

VER.03\_20171109



# FINGER PRINTER

REFERENCE:2200~2299



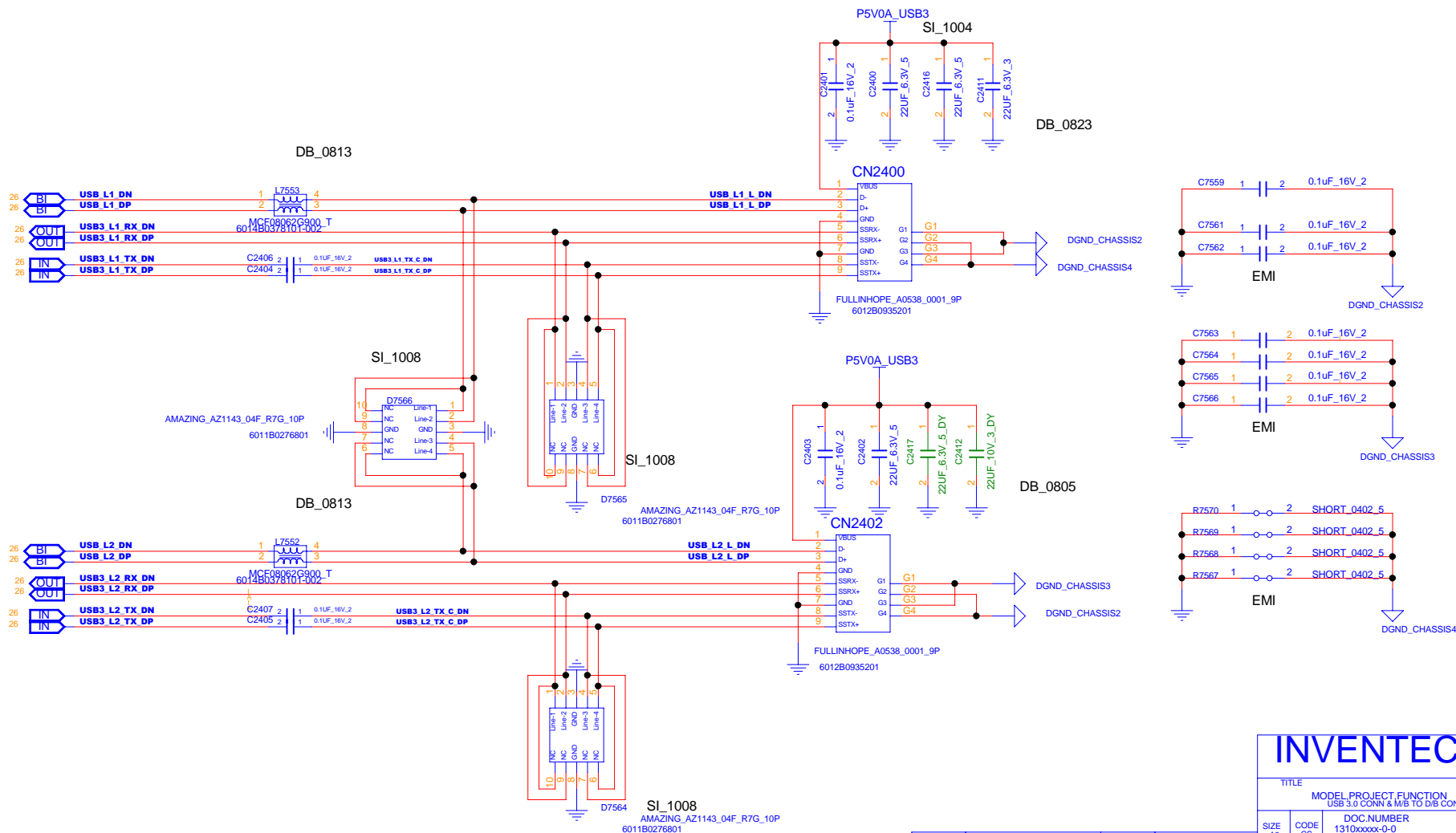
# INVENTEC

TITLE  
MODEL PROJECT FUNCTION  
Block Diagram

SIZE A3 CODE CS DOC NUMBER 1310xxxx-0-0 REV X01

SHEET 43 of 75

VER.08\_20171119

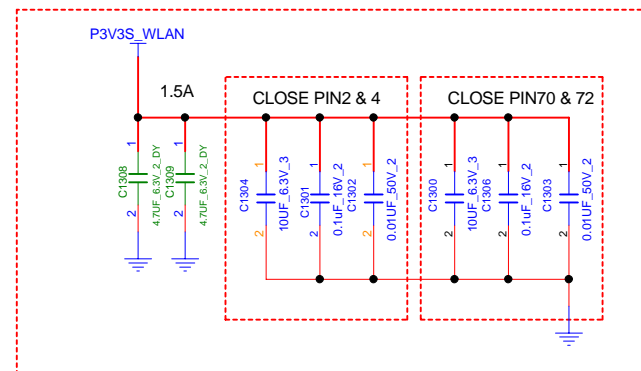


SIZE	CODE	DESCRIPTION
10	00	1310xxxxx-0-0

CHANGE by	XXX		DATE		SIZE A3	CODE CS	1310xxxx-0-0	X01
PCB P/N	6XXXXXX		PCB VER	VER A - 2002	SHEET	of 44	75	

D

DB\_0723



1

0

1

A

VER.05\_20171116



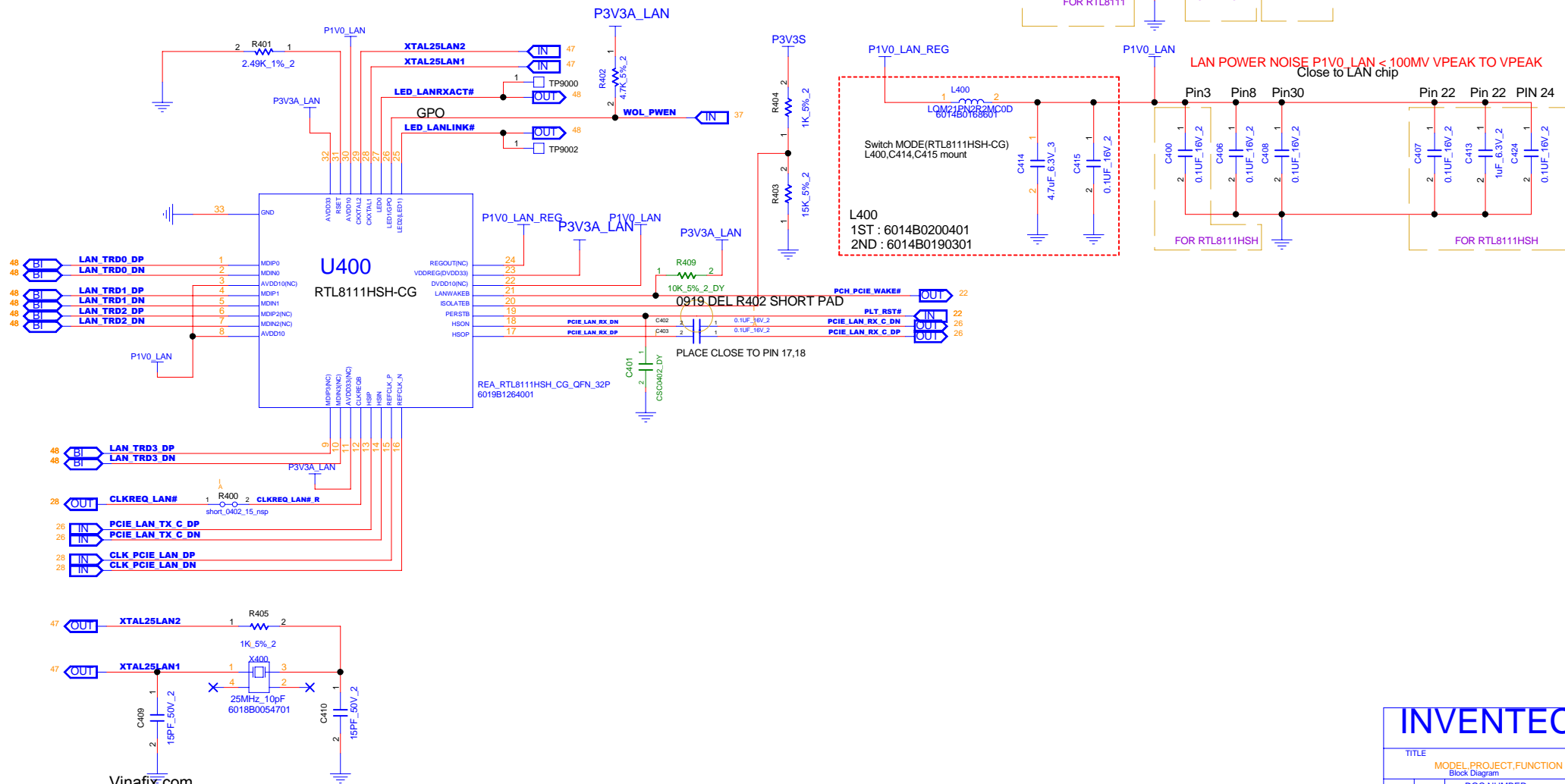
INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION AUDIO CODEC			
SIZE A3	CODE CS	DOC. NUMBER 1310xxxxx-0-0	REV X01
SHEET 46 of 75			

Location 400 ~ 469  
VER.05\_20171115-2

VER.05\_20171115-2

★ 6019B1264001	RTL8111HSH-CGT	10/100/1000
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Vinafix.com

INVENTEC

TITLE	MODEL.PROJECT.FUNCTION
1.1	1.1
1.2	1.2
1.3	1.3
1.4	1.4
1.5	1.5
1.6	1.6
1.7	1.7
1.8	1.8
1.9	1.9
1.10	1.10
1.11	1.11
1.12	1.12
1.13	1.13
1.14	1.14
1.15	1.15
1.16	1.16
1.17	1.17
1.18	1.18
1.19	1.19
1.20	1.20
1.21	1.21
1.22	1.22
1.23	1.23
1.24	1.24
1.25	1.25
1.26	1.26
1.27	1.27
1.28	1.28
1.29	1.29
1.30	1.30
1.31	1.31
1.32	1.32
1.33	1.33
1.34	1.34
1.35	1.35
1.36	1.36
1.37	1.37
1.38	1.38
1.39	1.39
1.40	1.40
1.41	1.41
1.42	1.42
1.43	1.43
1.44	1.44
1.45	1.45
1.46	1.46
1.47	1.47
1.48	1.48
1.49	1.49
1.50	1.50
1.51	1.51
1.52	1.52
1.53	1.53
1.54	1.54
1.55	1.55
1.56	1.56
1.57	1.57
1.58	1.58
1.59	1.59
1.60	1.60
1.61	1.61
1.62	1.62
1.63	1.63
1.64	1.64
1.65	1.65
1.66	1.66
1.67	1.67
1.68	1.68
1.69	1.69
1.70	1.70
1.71	1.71
1.72	1.72
1.73	1.73
1.74	1.74
1.75	1.75
1.76	1.76
1.77	1.77
1.78	1.78
1.79	1.79
1.80	1.80
1.81	1.81
1.82	1.82
1.83	1.83
1.84	1.84
1.85	1.85
1.86	1.86
1.87	1.87
1.88	1.88
1.89	1.89
1.90	1.90
1.91	1.91
1.92	1.92
1.93	1.93
1.94	1.94
1.95	1.95
1.96	1.96
1.97	1.97
1.98	1.98
1.99	1.99
2.00	2.00
2.01	2.01
2.02	2.02
2.03	2.03
2.04	2.04
2.05	2.05
2.06	2.06
2.07	2.07
2.08	2.08
2.09	2.09
2.10	2.10
2.11	2.11
2.12	2.12
2.13	2.13
2.14	2.14
2.15	2.15
2.16	2.16
2.17	2.17
2.18	2.18
2.19	2.19
2.20	2.20
2.21	2.21
2.22	2.22
2.23	2.23
2.24	2.24
2.25	2.25
2.26	2.26
2.27	2.27
2.28	2.28
2.29	2.29
2.30	2.30
2.31	2.31
2.32	2.32
2.33	2.33
2.34	2.34
2.35	2.35
2.36	2.36
2.37	2.37
2.38	2.38
2.39	2.39
2.40	2.40
2.41	2.41
2.42	2.42
2.43	2.43
2.44	2.44
2.45	2.45
2.46	2.46
2.47	2.47
2.48	2.48
2.49	2.49
2.50	2.50
2.51	2.51

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET		47 of 75	

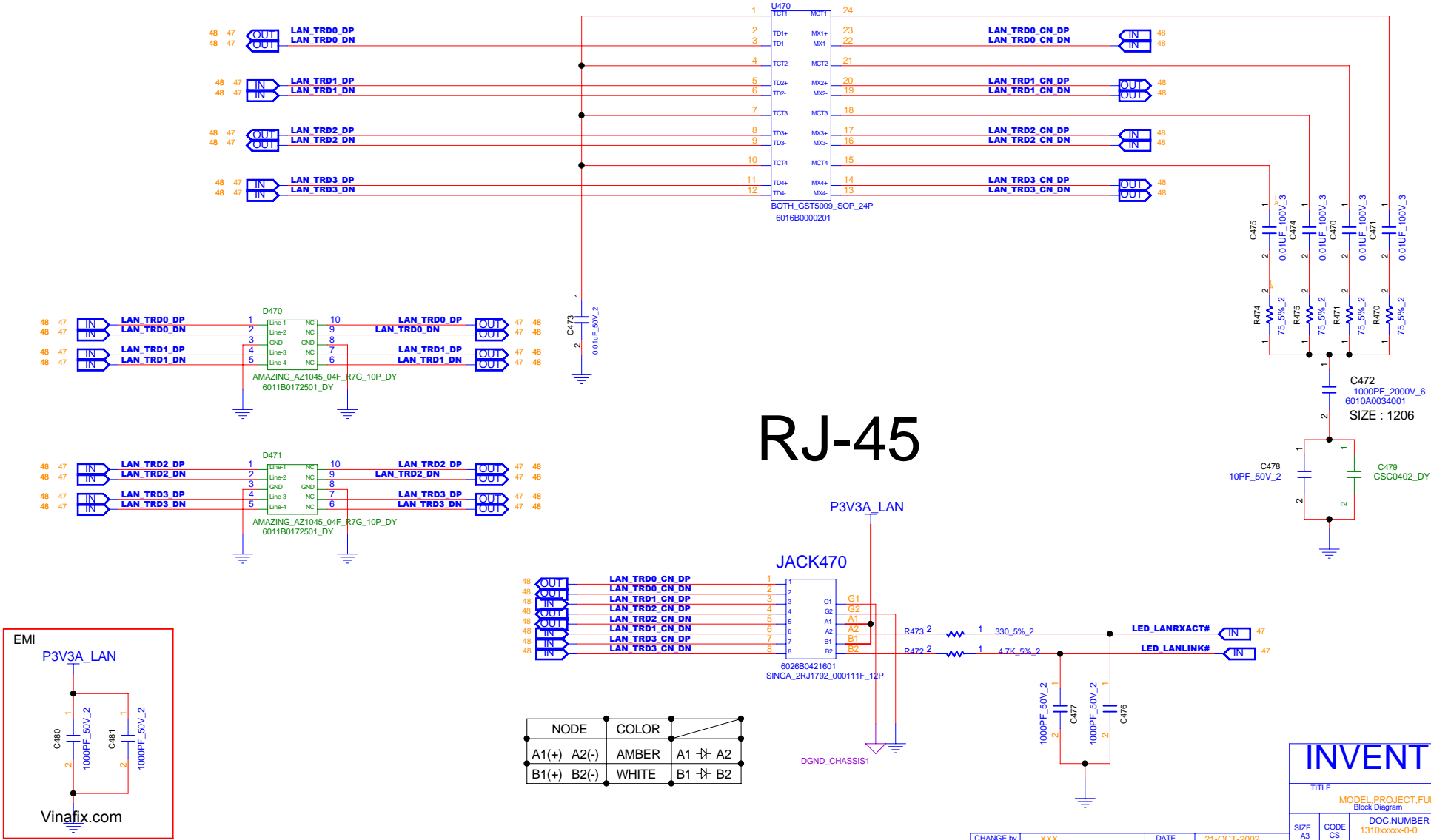
CHANGE by	XXX	DATE	21-OCT-2007
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

LAN (Transformer & RJ45)

Location 470 ~ 499  
VER.05\_20171107

For 10/100/1000 LAN      GIGA main BOM change to 6016B0000201  
10/100/1000 MAIN====> BOTHHAND P/N : 6016B0000201 GST5009  
10/100/1000 2ND====> UDE P/N : 6016B0022201 L22N001-0

RJ-45



INVENTEC

TITLE  
MODEL PROJECT FUNCTION

SIZE A3 CODE CS DOC NUMBER 1310xxxx-0-0 REV X01

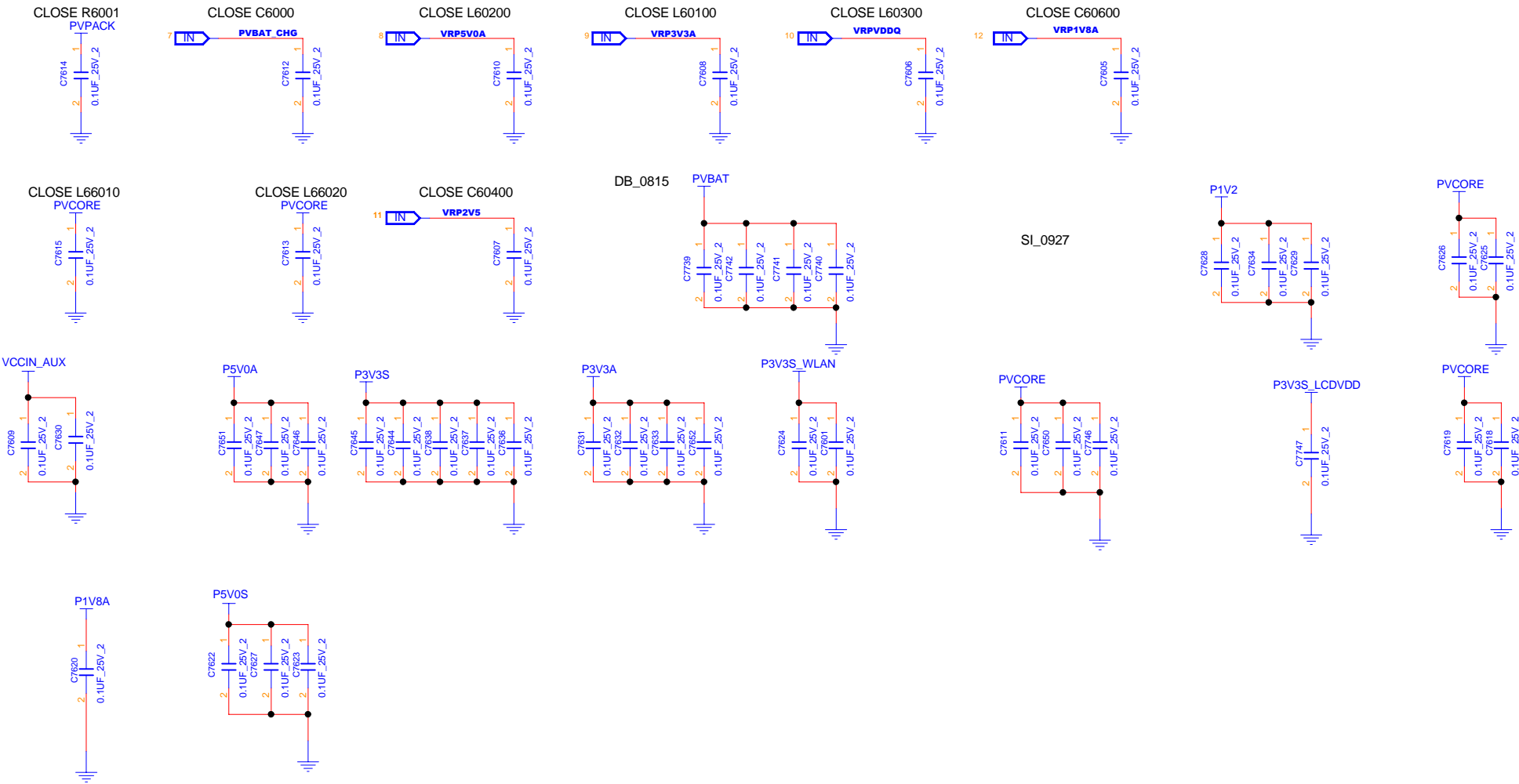
CHANGE by XXX DATE 21-OCT-2002  
PCB P/N 60xxxxxxx PCB VER XXX

SHEET 48 of 75



# EMI SOLUTION

LOCATION : 7600 - 7699



## LOCATION: 7500 - 7599



# INVENTEC

TITLE	MODEL,PROJECT,FUNCTION
1.1	1.1.1
1.2	1.2.1
1.3	1.3.1
1.4	1.4.1
1.5	1.5.1
1.6	1.6.1
1.7	1.7.1
1.8	1.8.1
1.9	1.9.1
1.10	1.10.1
1.11	1.11.1
1.12	1.12.1
1.13	1.13.1
1.14	1.14.1
1.15	1.15.1
1.16	1.16.1
1.17	1.17.1
1.18	1.18.1
1.19	1.19.1
1.20	1.20.1
1.21	1.21.1
1.22	1.22.1
1.23	1.23.1
1.24	1.24.1
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1.26	1.26.1
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1.30	1.30.1
1.31	1.31.1
1.32	1.32.1
1.33	1.33.1
1.34	1.34.1
1.35	1.35.1
1.36	1.36.1
1.37	1.37.1
1.38	1.38.1
1.39	1.39.1
1.40	1.40.1
1.41	1.41.1
1.42	1.42.1
1.43	1.43.1
1.44	1.44.1
1.45	1.45.1
1.46	1.46.1
1.47	1.47.1
1.48	1.48.1
1.49	1.49.1
1.50	1.50.1
1.51	1.51.1
1.52	1.52.1
1.53	1.53.1
1.54	1.54.1
1.55	1.55.1
1.56	1.56.1
1.57	1.57.1
1.58	1.58.1
1.59	1.59.1
1.60	1.60.1
1.61	1.61.1
1.62	1.62.1
1.63	1.63.1
1.64	1.64.1
1.65	1.65.1
1.66	1.66.1
1.67	1.67.1
1.68	1.68.1
1.69	1.69.1
1.70	1.70.1
1.71	1.71.1
1.72	1.72.1
1.73	1.73.1
1.74	1.74.1
1.75	1.75.1
1.76	1.76.1
1.77	1.77.1
1.78	1.78.1
1.79	1.79.1
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1.81	1.81.1
1.82	1.82.1
1.83	1.83.1
1.84	1.84.1
1.85	1.85.1
1.86	1.86.1
1.87	1.87.1
1.88	1.88.1
1.89	1.89.1
1.90	1.90.1
1.91	1.91.1
1.92	1.92.1
1.93	1.93.1
1.94	1.94.1
1.95	1.95.1
1.96	1.96.1
1.97	1.97.1
1.98	1.98.1
1.99	1.99.1
2.00	2.00.1
2.01	2.01.1
2.02	2.02.1
2.03	2.03.1
2.04	2.04.1
2.05	2.05.1
2.06	2.06.1
2.07	2.07.1
2.08	2.08.1
2.09	2.09.1
2.10	2.10.1
2.11	2.11.1
2.12	2.12.1
2.13	2.13.1
2.14	2.14.1
2.15	2.15.1
2.16	2.16.1
2.17	2.17.1
2.18	2.18.1
2.19	2.19.1
2.20	2.20.1
2.21	2.21.1
2.22	2.22.1
2.23	2.23.1
2.24	2.24.1
2.25	2.25.1
2.26	2.26.1
2.27	2.27.1
2.28	2.28.1
2.29	2.29.1
2.30	2.30.1
2.31	2.31.1
2.32	2.32.1
2.33	2.33.1
2.34	2.34.1
2.35	2.35.1
2.36	2.36.1
2.37	2.37.1
2.38	2.38.1
2.39	2.39.1
2.40	2.40.1
2.41	

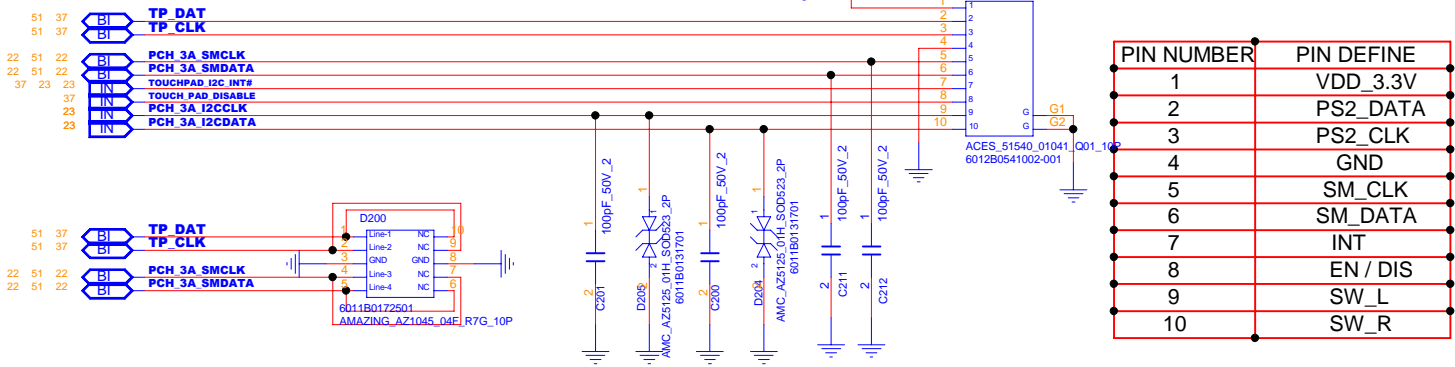
SIZE A3	CODE CS	DOC. NUMBER 1310xxxxx-0-0	REV X01
SHEET 50 of 75			

CHANGE by	XXX	DATE	21-OCT-2007
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

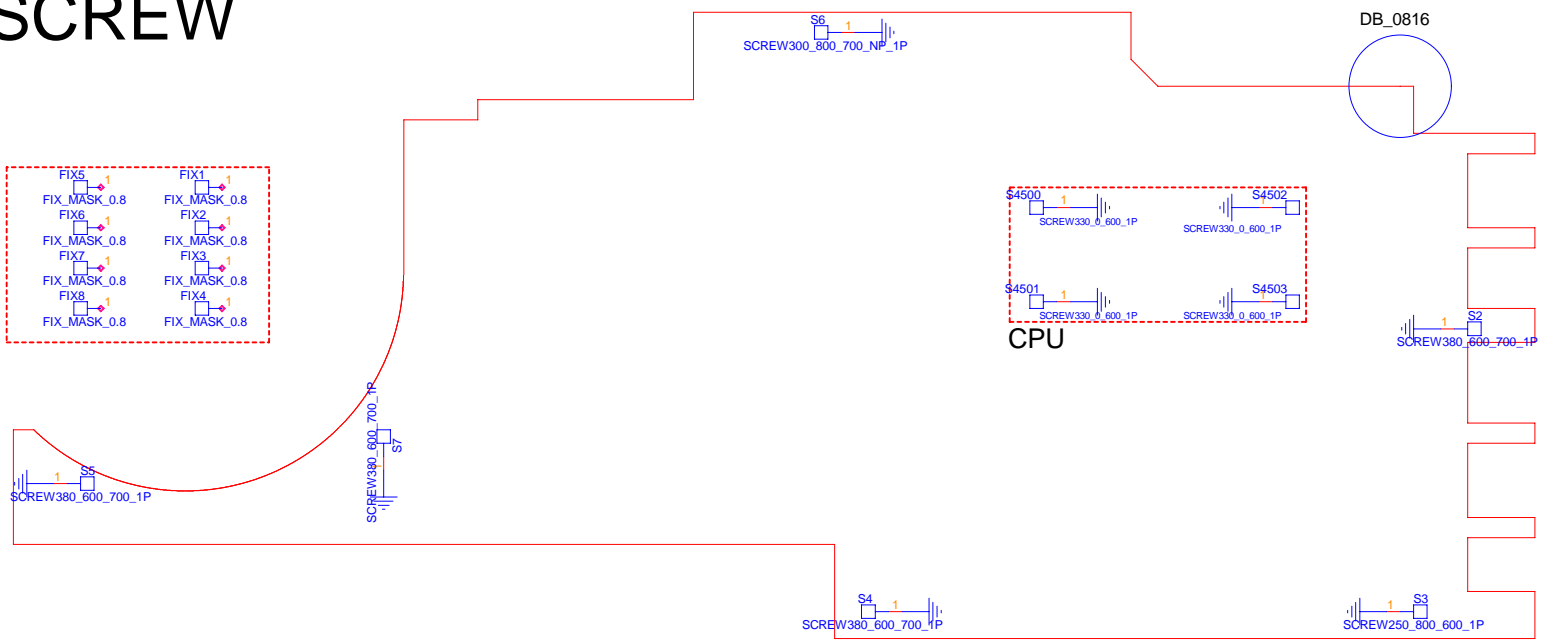
# TOUCHPAD MODULE CONN

## FOR INTEL USE

VER.14\_20171119



# SCREW



INVENTEC

TITLE  
MODEL PROJECT FUNCTION  
POWER BUTTON

SIZE A3 CODE CS DOC NUMBER 1310xxxx-0-0 REV X01

CHANGE by XXX DATE PCB VER XXX PCB VER XXX

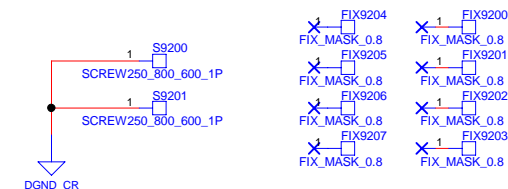
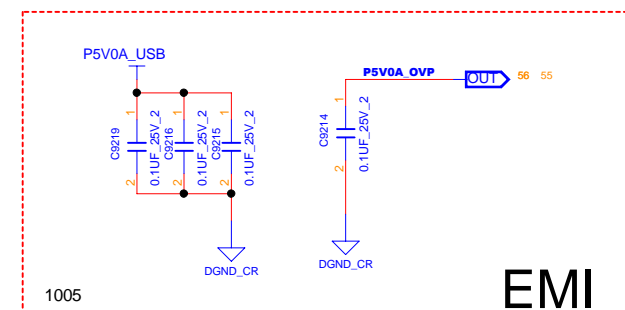
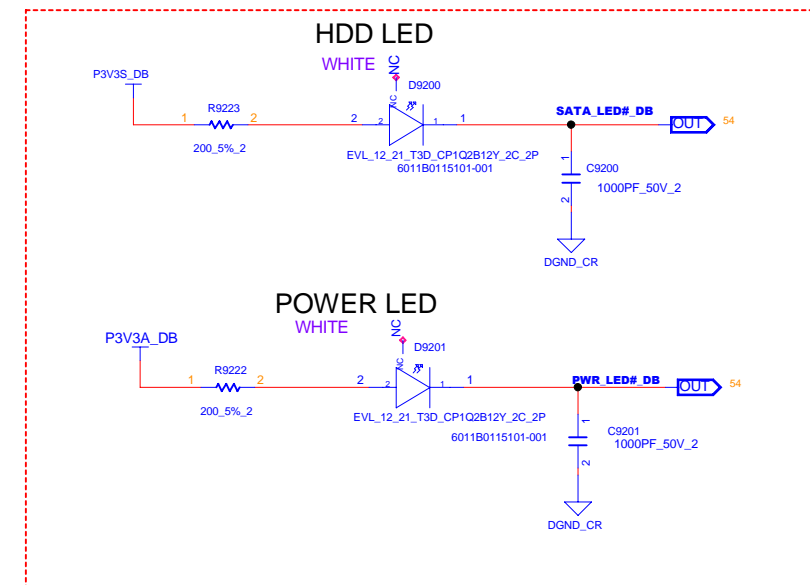
SHEET of 51 75



# Small Board

- 1.USB & CR FOR NARROW BORDER (LOCATION : 9200)
- 2.USB & CR FOR STANDARD BORDER (LOCATION : 9600)
3. PICK BUTTON BOARD (LOCATION : 9300)

VER.09\_20171109

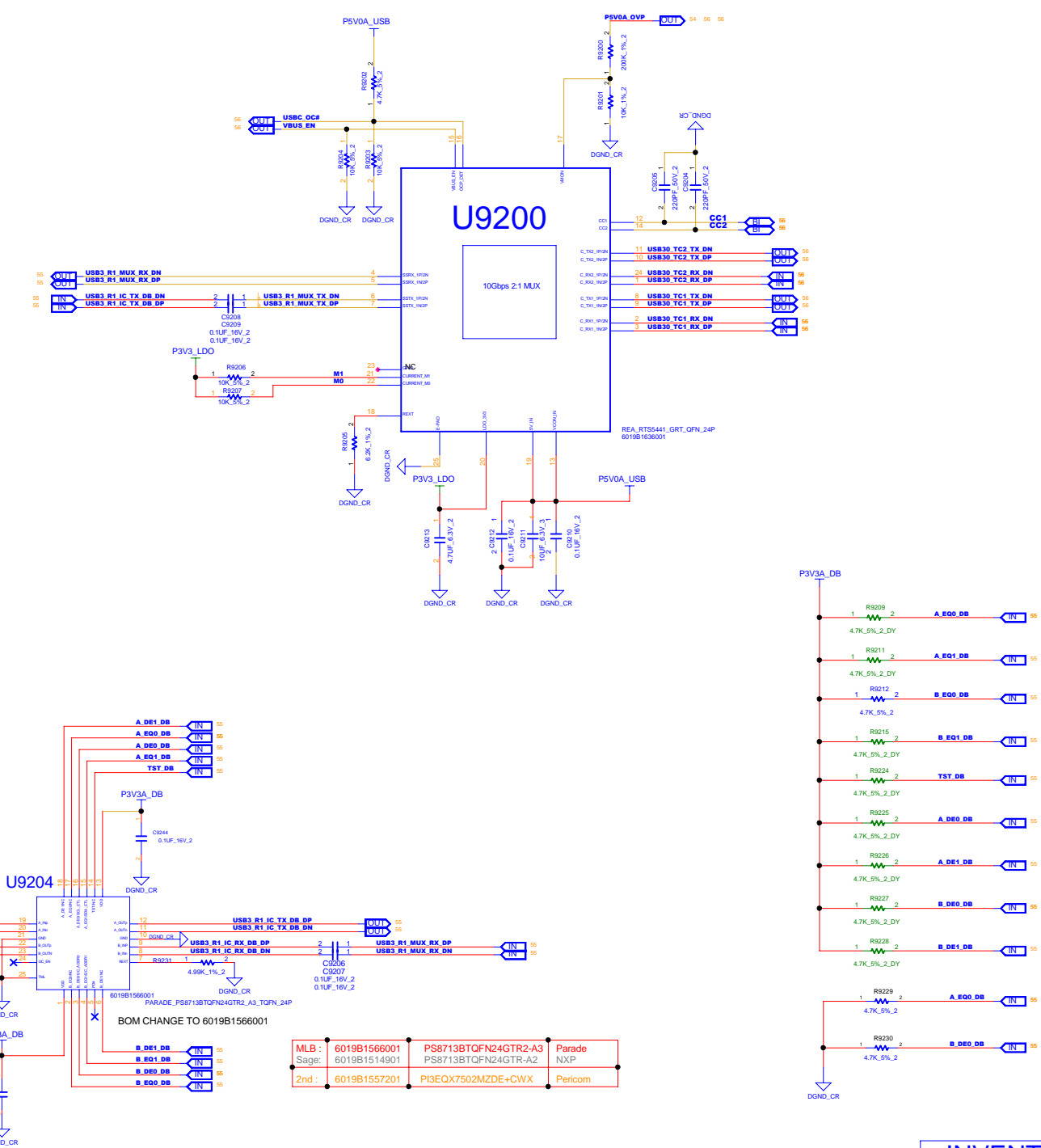


## INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET <i>of 54</i> <i>75</i>			

# USB3.0 MUX

FOR NARROW BORDER USE  
VER.02\_20170919



VER.13\_20171119





## D

C

B

A



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E

1

CHANGE by	XENG>	DATE	21-OCT-2002	SIZE	A3	CODE	CS	1310xxxxx-0-0	X01
PCB P/N	60xxxxxxxxxxx	PCB VER	XVER>	SHEET	57	of	75		

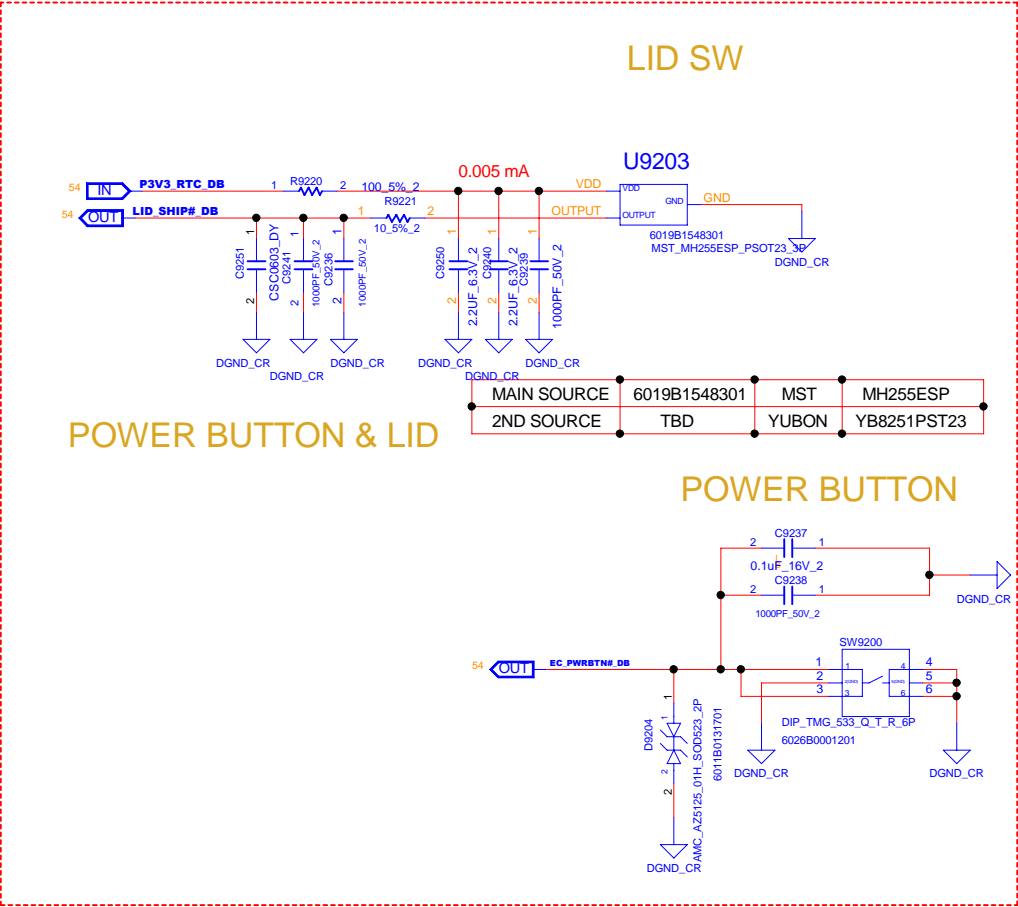
TITLE	MODEL,PROJECT,FUNCTION
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1.3	1.3.1
1.4	1.4.1
1.5	1.5.1
1.6	1.6.1
1.7	1.7.1
1.8	1.8.1
1.9	1.9.1
1.10	1.10.1
1.11	1.11.1
1.12	1.12.1
1.13	1.13.1
1.14	1.14.1
1.15	1.15.1
1.16	1.16.1
1.17	1.17.1
1.18	1.18.1
1.19	1.19.1
1.20	1.20.1
1.21	1.21.1
1.22	1.22.1
1.23	1.23.1
1.24	1.24.1
1.25	1.25.1
1.26	1.26.1
1.27	1.27.1
1.28	1.28.1
1.29	1.29.1
1.30	1.30.1
1.31	1.31.1
1.32	1.32.1
1.33	1.33.1
1.34	1.34.1
1.35	1.35.1
1.36	1.36.1
1.37	1.37.1
1.38	1.38.1
1.39	1.39.1
1.40	1.40.1
1.41	1.41.1
1.42	1.42.1
1.43	1.43.1
1.44	1.44.1
1.45	1.45.1
1.46	1.46.1
1.47	1.47.1
1.48	1.48.1
1.49	1.49.1
1.50	1.50.1
1.51	1.51.1
1.52	1.52.1
1.53	1.53.1
1.54	1.54.1
1.55	1.55.1
1.56	1.56.1
1.57	1.57.1
1.58	1.58.1
1.59	1.59.1
1.60	1.60.1
1.61	1.61.1
1.62	1.62.1
1.63	1.63.1
1.64	1.64.1
1.65	1.65.1
1.66	1.66.1
1.67	1.67.1
1.68	1.68.1
1.69	1.69.1
1.70	1.70.1
1.71	1.71.1
1.72	1.72.1
1.73	1.73.1
1.74	1.74.1
1.75	1.75.1
1.76	1.76.1
1.77	1.77.1
1.78	1.78.1
1.79	1.79.1
1.80	1.80.1
1.81	1.81.1
1.82	1.82.1
1.83	1.83.1
1.84	1.84.1
1.85	1.85.1
1.86	1.86.1
1.87	1.87.1
1.88	1.88.1
1.89	1.89.1
1.90	1.90.1
1.91	1.91.1
1.92	1.92.1
1.93	1.93.1
1.94	1.94.1
1.95	1.95.1
1.96	1.96.1
1.97	1.97.1
1.98	1.98.1
1.99	1.99.1
2.00	2.00.1
2.01	2.01.1
2.02	2.02.1
2.03	2.03.1
2.04	2.04.1
2.05	2.05.1
2.06	2.06.1
2.07	2.07.1
2.08	2.08.1
2.09	2.09.1
2.10	2.10.1
2.11	2.11.1
2.12	2.12.1
2.13	2.13.1
2.14	2.14.1
2.15	2.15.1
2.16	2.16.1
2.17	2.17.1
2.18	2.18.1
2.19	2.19.1
2.20	2.20.1
2.21	2.21.1
2.22	2.22.1
2.23	2.23.1
2.24	2.24.1
2.25	2.25.1
2.26	2.26.1
2.27	2.27.1
2.28	2.28.1
2.29	2.29.1
2.30	2.30.1
2.31	2.31.1
2.32	2.32.1
2.33	2.33.1
2.34	2.34.1
2.35	2.35.1
2.36	2.36.1
2.37	2.37.1
2.38	2.38.1
2.39	2.39.1
2.40	2.40.1
2.41	

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 57 of 75			

# LID SW & POWER BUTTON

FOR NARROW BORDER USE

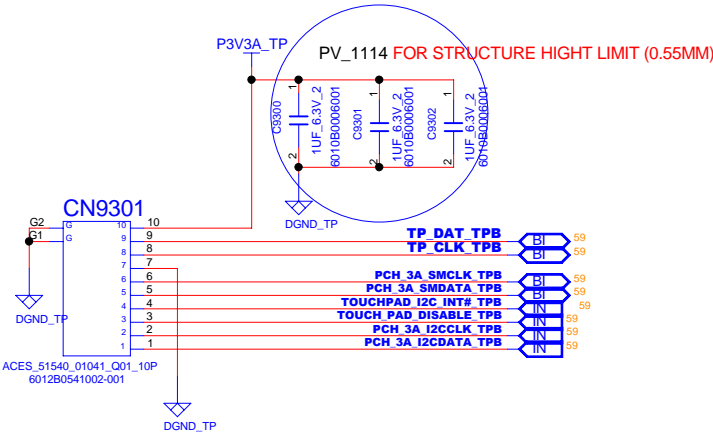
VER.07\_20171120



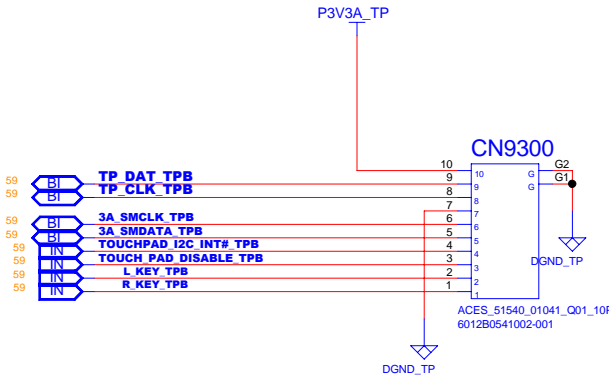
# PICK BUTTON (TYPE\_C)

## TOUCHPAD R / L BOARD

VER.03\_20171119

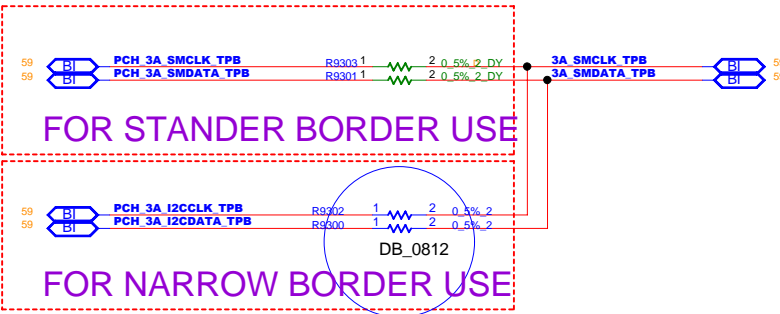


TO MAIN BOARD



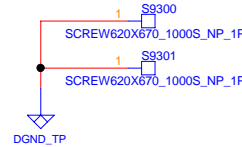
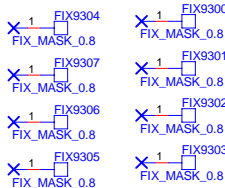
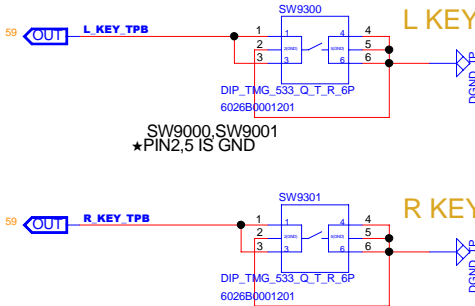
TO TP MODULE

PIN DEFINE	PIN NUMBER
VDD_3.3V	1
PS2_DATA	2
PS2_CLK	3
GND	4
SM_CLK	5
SM_DATA	6
INT	7
EN / DIS	8
SW_L	9
SW_R	10



FOR STANDER BORDER USE

FOR NARROW BORDER USE



INVENTEC

TITLE	MODEL PROJECT FUNCTION	DOC NUMBER	REV
Block Diagram		1310xxxx-0-0	X01
SIZE A3	CODE CS	SHEET 59 of 75	

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NOTES:  
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

AMD R19M-M18/30 18W

GDDR52PCSX64BITX256MX32

2019.11.14

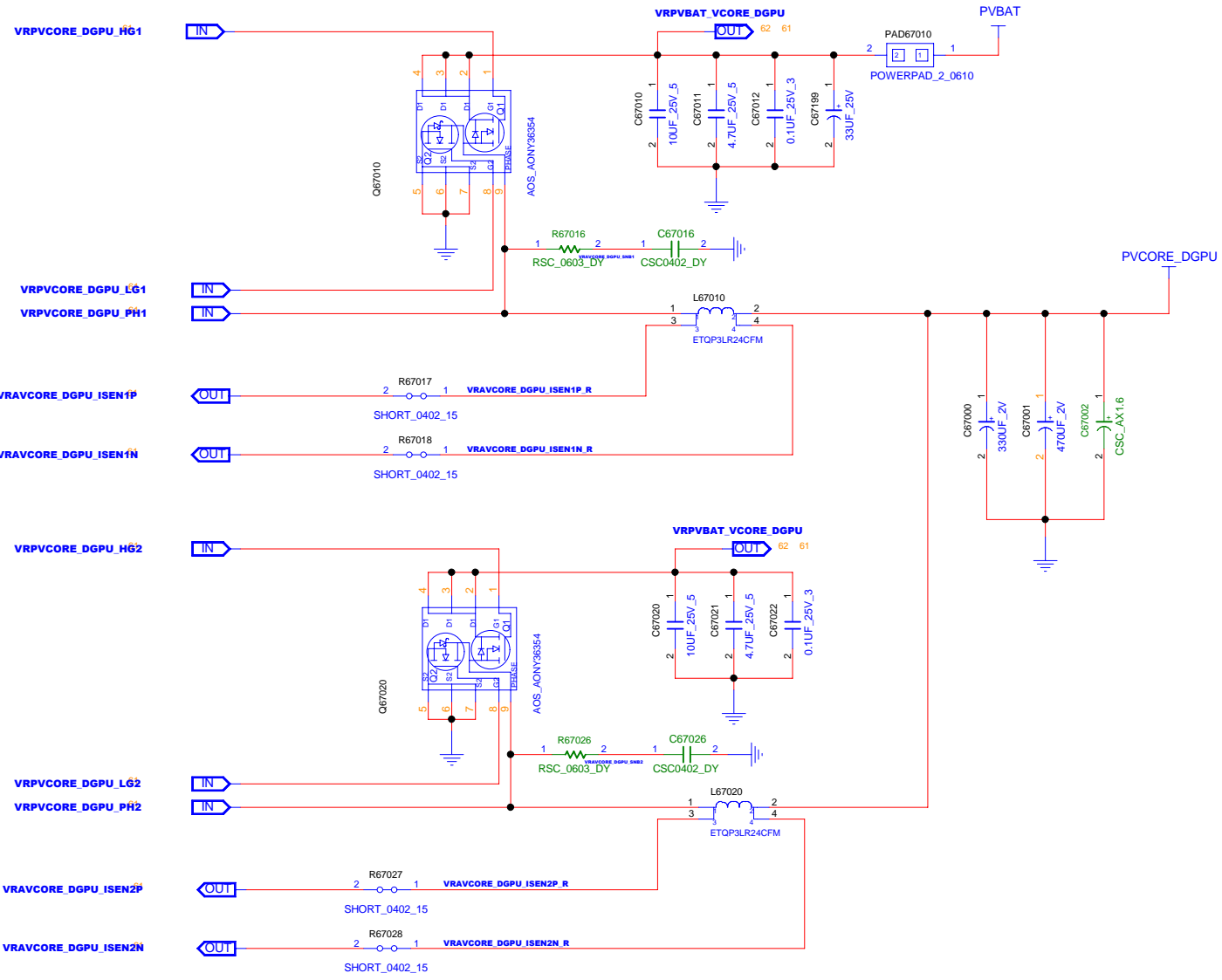
R19M-M18-30 PART NUMBER TABLE

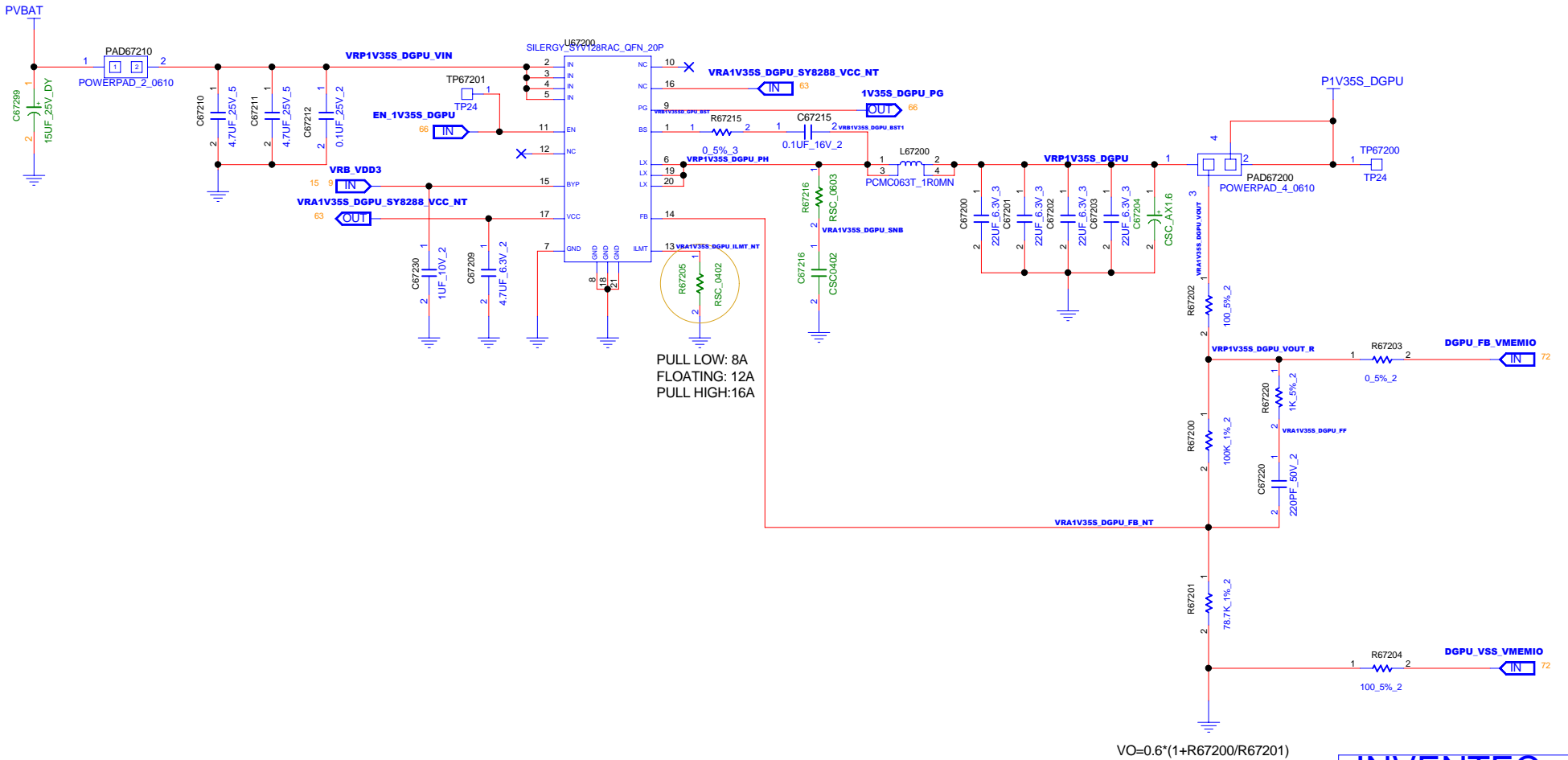
	U5001
M18-30	6019B1961001

R19M-M18-30 /70 BOOT VID

Boot-VID Code		
SVC	SVD	Voltage Selected (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8













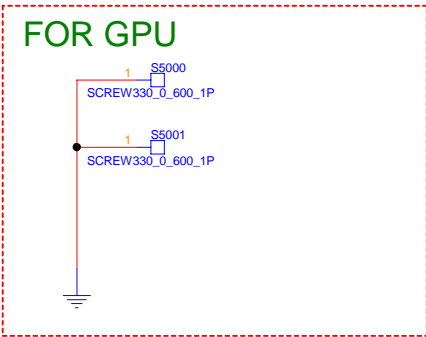
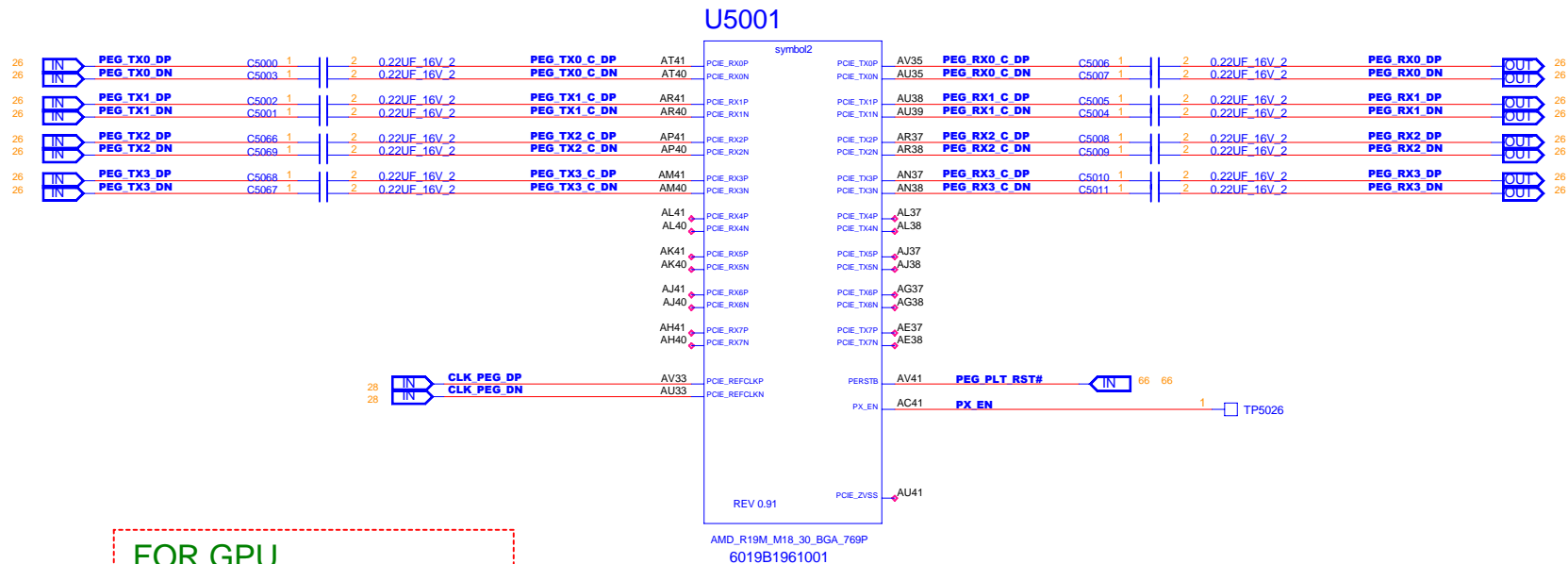
## A



# GPU PCI-E

U5001  
R19M-M18-30  
216-0915020  
6019B1961001

PLEASE NOTE!! THIS SYMBOL IS THE SAME PIN DEFINE AS R19M-M18-70,BUT IT'S NOT R19M-M18-30.  
THE CIRCUIT STILL NEEDS TO REFER TO THE R19M-M18-30 SPECIFICATION

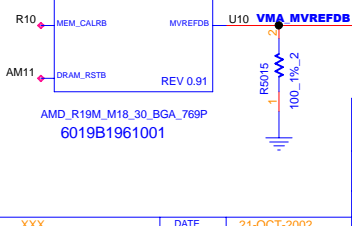
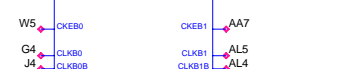
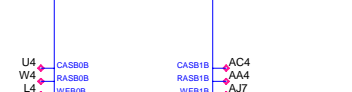
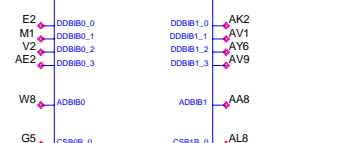
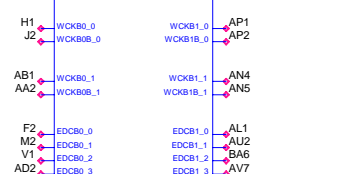
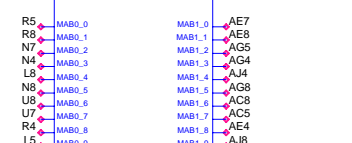
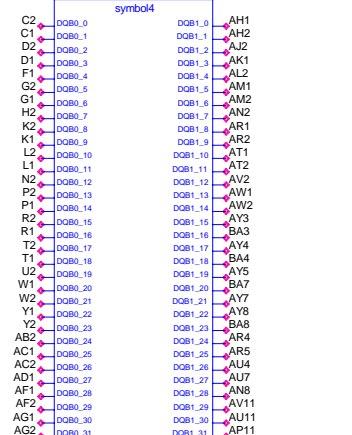
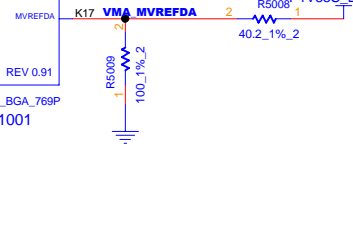
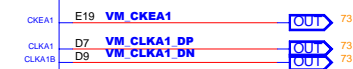
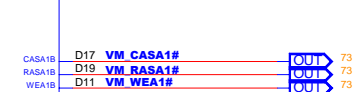
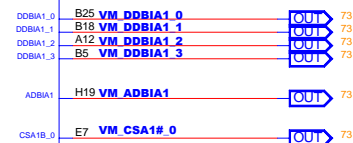
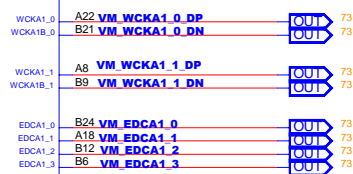
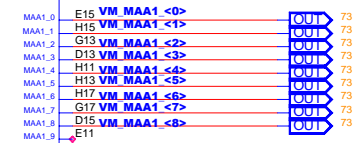
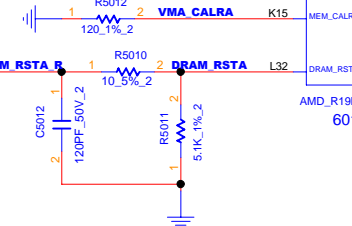
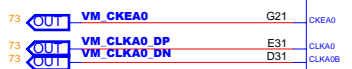
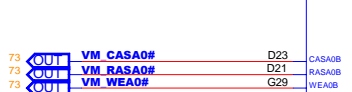
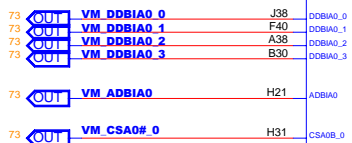
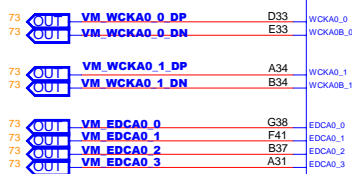
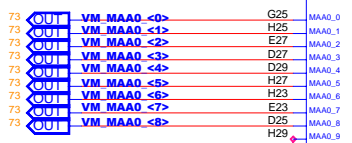
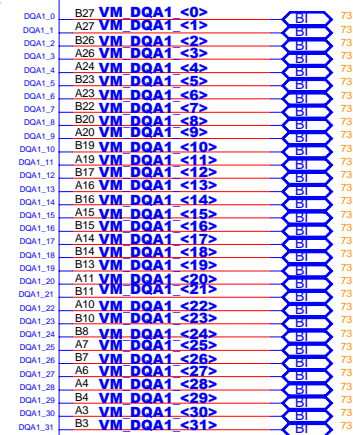
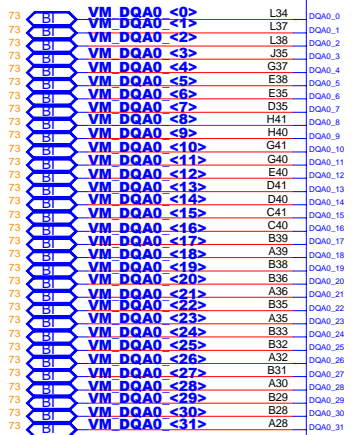


# GPU FRAME BUFFER A

U5001

U5001

# GPU FRAME BUFFER B



## INVENTEC

TITLE MODEL PROJECT FUNCTION POLARIS-2

SIZE CODE DOC NUMBER REV

A3 CS 1310xxxxx-0-0 X01

SHEET 68 of 75

CHANGE by XXX PCB P/N 60xxxxxxx DATE 21-OCT-2002 PCB VER XXX

Vinafix.com

AMD\_R19M\_M18\_30\_BGA\_769P 6019B1961001

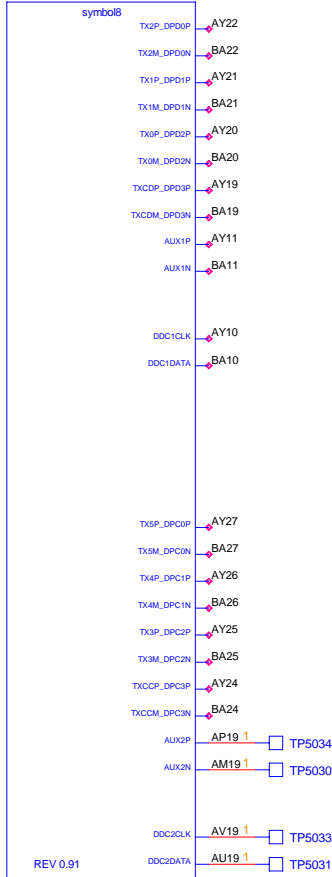
AMD\_R19M\_M18\_30\_BGA\_769P 6019B1961001

P1V35S\_DGPU

P1V35S\_DGPU

# GPU VGA / LVDS / DVI / HDMI / DP

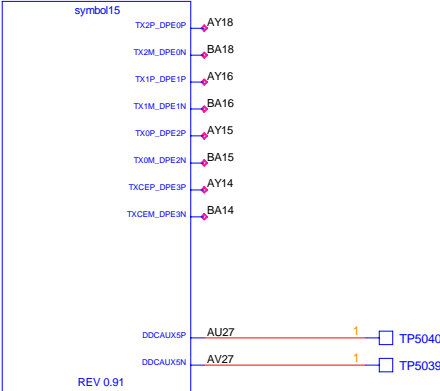
U5001



AMD\_R19M\_M18\_30\_BGA\_769P

6019B1961001

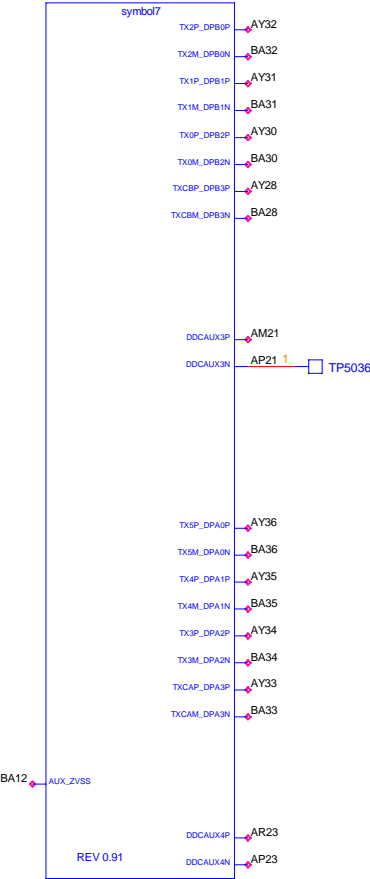
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AMD\_R19M\_M18\_30\_BGA\_769P

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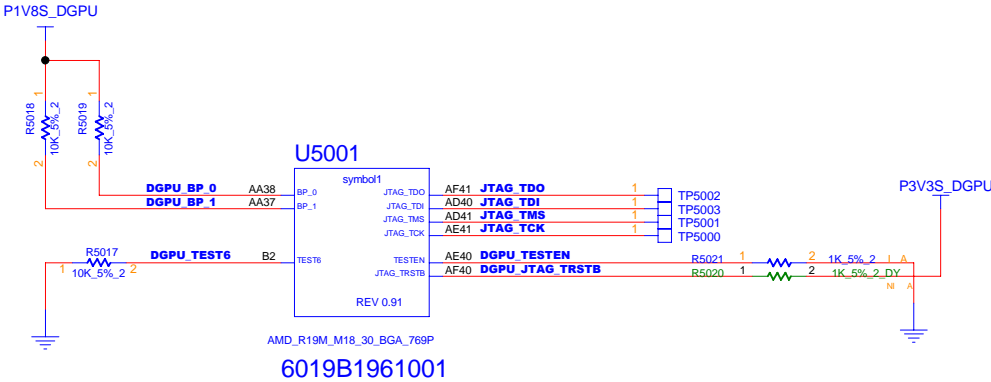
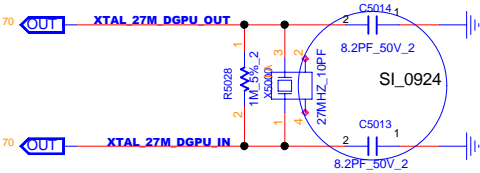
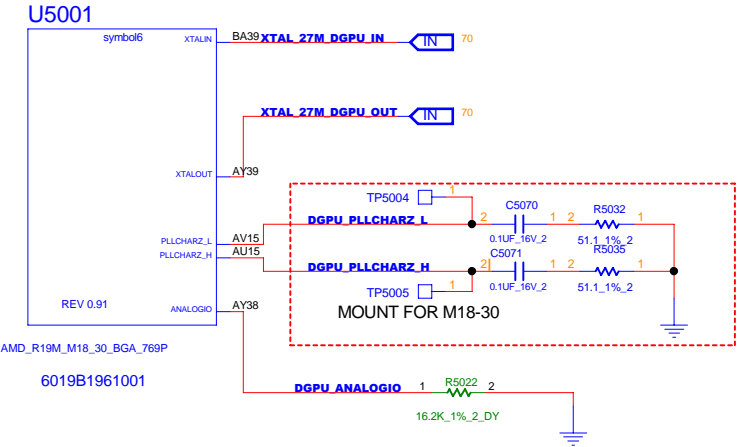
U5001



AMD\_R19M\_M18\_30\_BGA\_769P

6019B1961001

# GPU-CLOCK/JTAG



INVENTEC

TITLE

MODEL PROJECT FUNCTION

POLARIS-5

SIZE A3

CODE CS

DOC NUMBER 1310xxxx-0-0

REV X01

SHEET 70 of 75

CHANGE by XXX

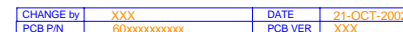
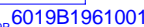
DATE 21-OCT-2002

PCB P/N 60xxxxxxxxxx

PCB VER XXX



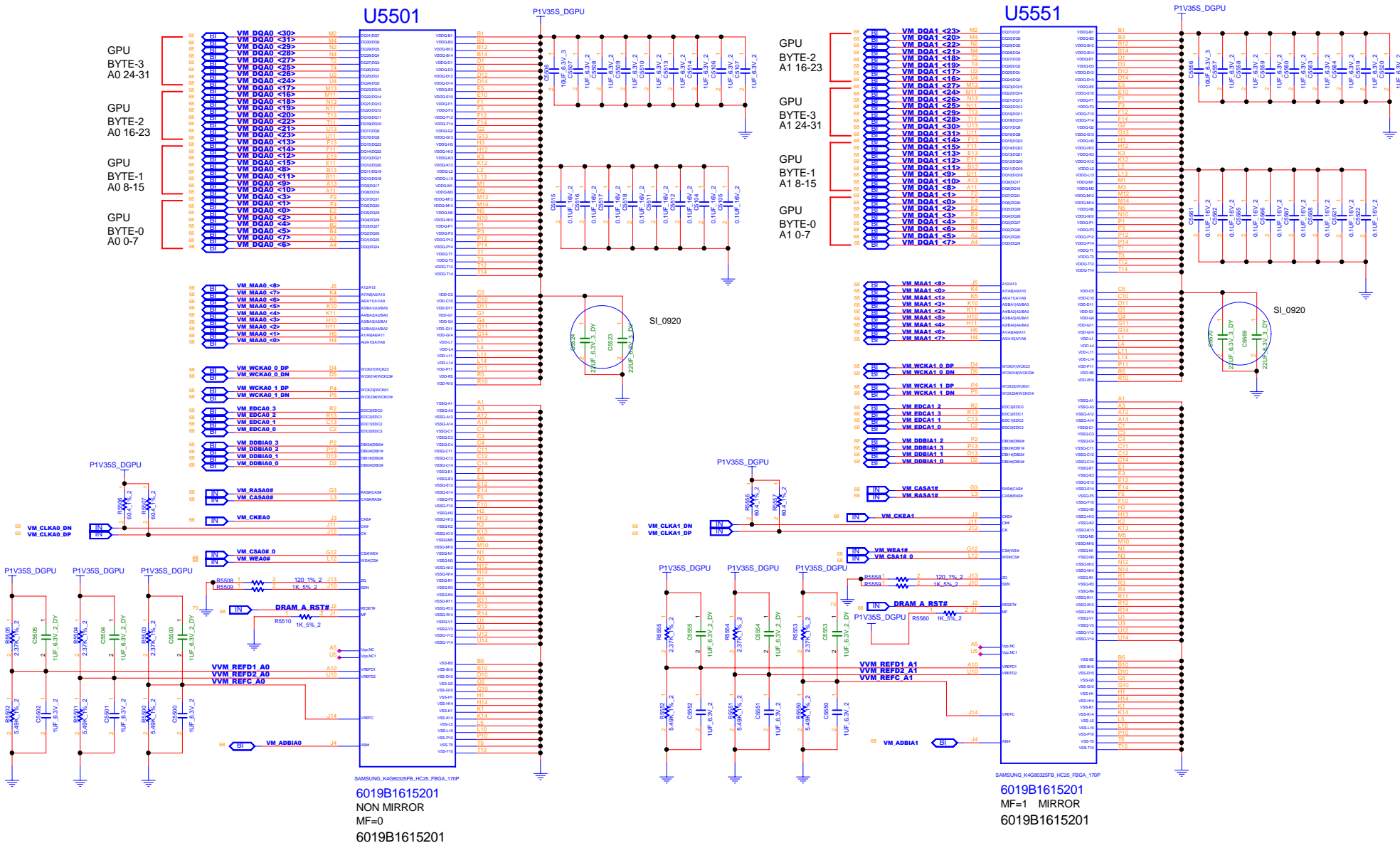
## A



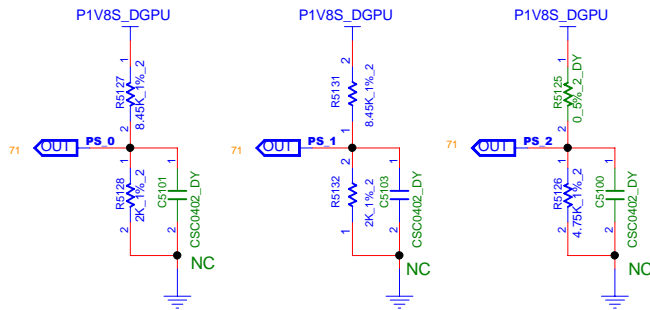
A3	CS	REVENUE 2
SHEET		72 of 75



# GDDR5 VRAM



# R19M-M18-30VVRAM ID



PS0[5:1]	1	1	0	0	1
PS1[5:1]	1	1	0	0	1
PS2[5:1]	1	1	0	0	0
PS3[5:1]	1	1	PS3[3]	PS3[2]	PS3[1]

APERTURE MEMORY SIZE IS 256K  
R5127 IS 8.45K OHM \ R5128 IS 2K OHM

MULTI LEVEL PIN STRAP (MLPS)  
FOR R\_PU\_X AND R\_PD\_X AND C\_X SELECTION  
REFER TO AN.MEN.X1  
PARTS FOR MLPS SHOULD BE PLACED CLOSE TO ASIC  
THE TOTAL RESISTANCE OF TRACE SHOULD BE LESS THAN 3 OHM

R_PU	R_PD	BITS[3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

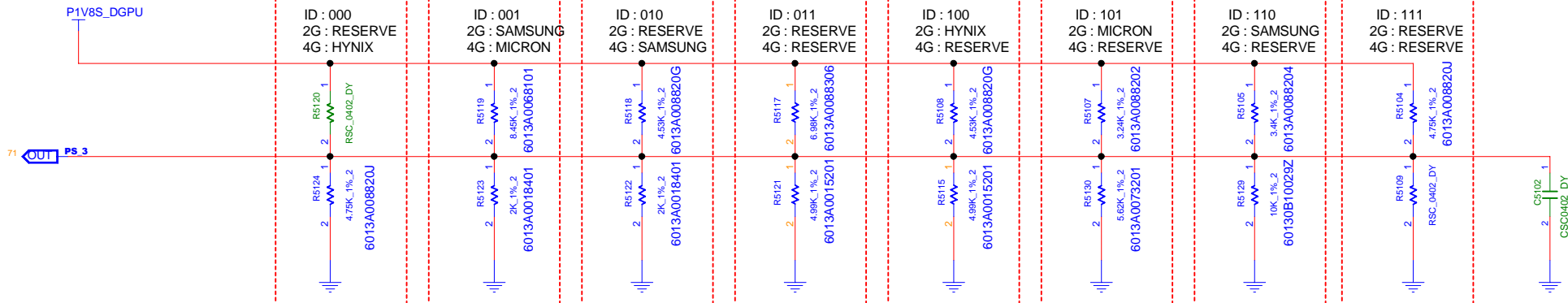
2K\_1% : 6013A0018401  
3.24K\_1% : 6013A0088202  
3.4K\_1% : 6013A0088204  
4.53K\_1% : 6013A008820G  
4.75K\_1% : 6013A008820J  
4.99K\_1% : 6013A0015201  
5.62K\_1% : 6013A0073201  
6.98K\_1% : 6013A0088306  
8.45K\_1% : 6013A0068101  
10K\_1% : 60130B10029Z

NOTE: 0402 1% RESISTORS ARE REQUIRED.

CAPACITOR VALUE (NF)	BITS [5:4]
680	00
82	01
10	10
NC	11

R5120 , R5119 , R5118 , R5117 , R5108 , R5107 , R5105 , R5104  
ARE COLAY WITH SAME POSITION

R5124 , R5123 , R5122 , R5121 , R5115 , R5130 , R5129 , R5109  
ARE COLAY WITH SAME POSITION

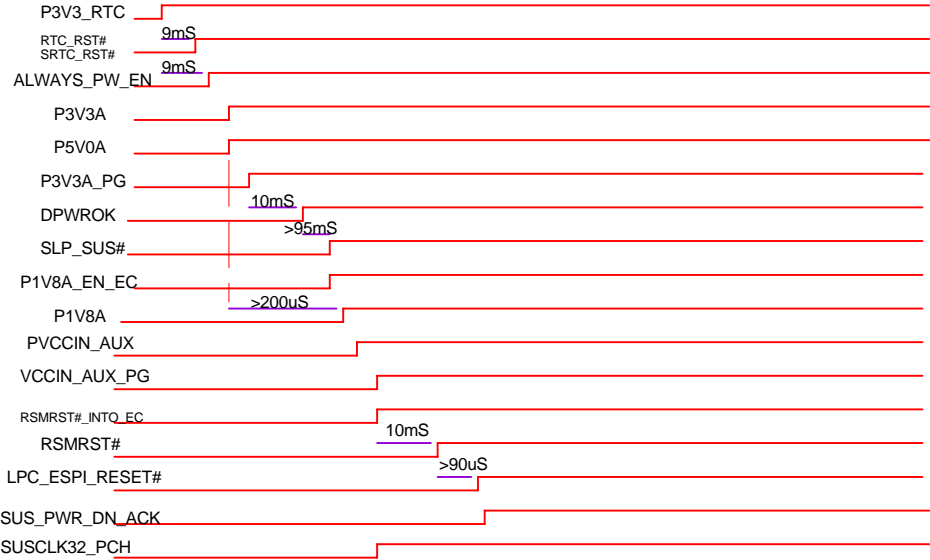


VRAM ID TABLE (256M X 32) TWO PIECES CHIP

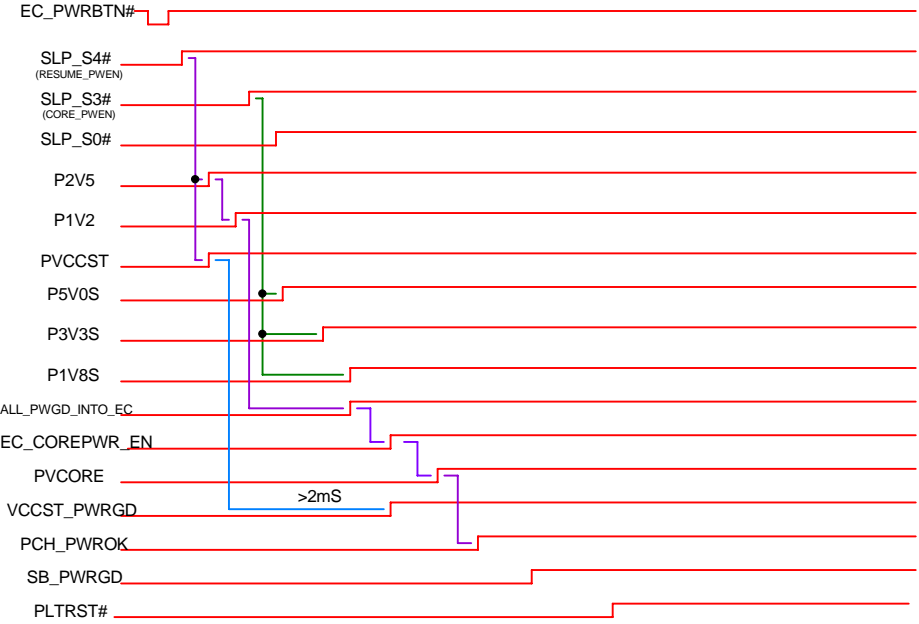
R_PU	R_PD	PS_3[3]	PS_3[2]	PS_3[1]	VENDER	IEC P/N	CONFIGURATION	VENDER P/N
NC (R5120)	4.75K (R5124)	0	0	0	RESERVE		256M X 32	
8.45K (R5119)	2K (R5123)	0	0	1	Samsung	6019B1926601	256M X 32	K4G80325FC-HC25 *
4.53K (R5118)	2K (R5122)	0	1	0	RESERVE		256M X 32	
6.98K (R5117)	4.99K (R5121)	0	1	1	Micron	6019B1721101	256M X 32	MT51J256M32HF-80:B B *
4.53K (R5108)	4.99K (R5115)	1	0	0	Hynix	6019B1542101 6019B1615301	256M X 32	H5GC8H24MJR-R0C H5GQ8H24MJR-R4C
3.24K (R5107)	5.62K (R5130)	1	0	1	Micron	6019B1486001	256M X 32	MT51J256M32HF-70:A
3.4K (R5105)	10K (R5129)	1	1	0	Samsung	6019B1485901 6019B1615201	256M X 32	K4G80325FB-HC28 K4G80325FB-HC25
4.75K (R5104)	NC (R5109)	1	1	1	Hynix	6019B1723701	256M X 32	H5GC8H24AJR-R2C A *

POWER SEQUENCE

G3 to S5



S5 to S0



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INVENTEC

TITLE  
MODEL,PROJECT,FUNCTION  
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002	SIZE	A3	CODE	CS	DOC NUMBER	1310xxxxx-0-0	REV	X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET	75	of	75				